Power-on domain #1

Power-on domain #2

Eliminated 1.5V off PCIe card due to inconsistent availability of 1.5V on adapters

Power-on domain #3

Power-on domain #4

Read UG482 for guidelines on decaps for Artix FPGA

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Configuration note:

1. CFGBVS on FPGA tied to 0V - VCCO_0 set to 1.5V
2. MCU must initialize GPIOs within 5ms of power on.
3. MCU holds SPI address pin HIGH for 290us minimum
4. MCU monitors DS0, reports status.

Note: MCU SPI pins remain Hi-Z at all times.

FPGA configuration should succeed even when MCU is unprogrammed (but SPI is programmed) due to pull-up on FPGA_DRIVE.

Update SPI ROM:
1. MCU disconnects FPGA by deasserting FPGA_DRIVE
2. MCU configures drive on SPI pins
3. Data arrives via USB and is written into SPI
4. MCU re-asserts SPI pins
5. MCU re-asserts FPGA by asserting FPGA_DRIVE
6. optional MCU re-asserts FPGA configuration by pulsing PROGRAM

If you must coordinate MCU pin state vs. optional external FPGA attachment.

PB0: Used for external SPI master.

PB3: Used for EXTERNAL SPI slave.
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HDMI ESD level shift

DDC SDA override circuit

SCL remap to SDA on this device to simplify BGA layout

SCL Override U"P

SCL Override D

HDMI ESD override circuit

Power from unused 5V supply to ESD 5V

4.7uF, 6.3V, X5R

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