1 ES8328E BLOCK DIAGRAM
INPUT SIGNAL PATH

The two analogue inputs LINPUT1/2 RINPUT1/2 can be selected by a switch, and then followed by a PGA gain boost. The inputs can be individually selected or a differential input of either (LINPUT1 RINPUT1) or (LINPUT2 RINPUT2) may also be selected. These inputs can be configured as microphone or line level. The signal then enters a high quality ADC. Alternatively, the two channels can also be mixed in the analogue domain and digitized in one ADC while the other ADC is turned off.

One on-chip ALC module can be used to control the signal level during recording. The gain of the PGA can be controlled either by the user or by the on-chip ALC function.

OUTPUT SIGNAL PATH

The output signal paths consist of digital filters, DACs, analogue mixers and output drivers. The digital filters and DACs are enabled in the “playback” or “record and playback” mode. In “bypass” mode, the analogue mixing and amplification can be utilized while DAC is disabled. DACs output can be mixed with analogue signals from the input pins Linput1/2 and Rinput1/2, and the mixed signal is fed to the output drivers LOUT1/ROUT1, LOUT2/ROUT2. The mixers and output drivers can be separately enabled by individual control bits.

The LOUT1/ROUT1 and LOUT2/ROUT2 can drive a 16Ω (up to 40mW) or 32Ω stereo headphone or stereo line output.

2 Recommended operating condition

<table>
<thead>
<tr>
<th>Digital supply range (Core)</th>
<th>DVDD</th>
<th>1.8V to 3.3V (Lowest power consumption at 1.8V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital supply range (Buffer)</td>
<td>PVDD</td>
<td>1.8V to 3.3V</td>
</tr>
<tr>
<td>Analog supply range</td>
<td>HPVDD, AVDD</td>
<td>1.8V to 3.3V (Best audio performance at 3.3V)</td>
</tr>
<tr>
<td>Ground</td>
<td>DGND, AGND, HPGND</td>
<td>0V</td>
</tr>
</tbody>
</table>
Typical Application Circuit

One LDO is recommended to provide power supply to ES8328.

The I2C chip address is 0x22 while pin CE is pull up to VDD.

The I2C chip address is 0x20 while pin CE is pull down to GND.
Notes:
* One LDO is recommended to provide power supply to ES8328E because ES8328E is an analog device which will be sensitive to noise.
* A differential Microphone circuit is recommended to ES8328E.
* The signal MIC_INP and MIC_INN must be parallel with each other on PCB layout.
* Filter and decoupling capacitors should be located as close to ES8328E package as possible during layout.
* Two 1K pull up resistors are recommended to I2C bus. R-C low pass filter is recommended to I2C CLK.
* If PIN26 (CE) be pulled down to GND, I2C Chip ID is 0x20, otherwise 0x22.
* One 10ohm resistor is recommended between AVDD and HPVDD if AVDD and HPVDD share the same power supply.

4 I2C / SPI Interface

I2C is a bi-directional bus which can be used to read or write register. SPI bus should only be used to write register.

**I2C BUS**

Don’t connect CE pin to IO of MCU, CPU or DSP. CE pin should be pulled up to PVDD or pulled down to DGND.

The chip address for I2C is 0x20 if CE pin is pulled down to DGND. The chip address for I2C is 0x22 if CE pin is pulled up to PVDD.

There are two pull-up resistors on I2C CCLK pin and I2C CDATA pin. 1KΩ resistor is recommended for the pull-up resistors.

![I2C timing](image)

**SPI BUS**

CE pin should be connected to IO of MCU, CPU or DSP. Don’t connect CE pin to DGND. The chip address for SPI is 0x20. SPI bus should only be used to write register.

![SPI DIN and CLK](image)

![Register Data Mapping](image)

5 Digital Audio Interface

The digital audio interface is used for inputting DAC data to ES8328E and outputting ADC data from it. The digital audio interface uses four pins:

**ASDOUT** : ADC data output
**DSDIN** : DAC data input
The clock signals SCLK and LRCK can be outputs when ES8328E operates as a master, or inputs when it is a slave.

ES8328E can support four different audio data formats:
- I2S
- Left Justified
- Right Justified
- DSP mode (PCM)

All four of these formats are MSB first.

5.1 Master and Slave Mode operation

ES8328E digital audio interface can operate as a master or a slave as shown in the figure listed below.

In master mode, SCLK is derived from MCLK via a programmable division set by BCLK_DIV. LRCK is derived from MCLK via a programmable division set by ADCFsRatio or DACFsRatio.

In slave mode, ES8328E can auto check MCLK/LRCK ratio and MCLK/SCLK ratio.

The Bit7(MSC) in register 0x08 should be used to set ES8328E in Master or Slave mode.

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSC</td>
<td>7</td>
<td>0 – slave serial port mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 – master serial port mode (default)</td>
</tr>
<tr>
<td>MCLKDIV2</td>
<td>6</td>
<td>0 – MCLK not divide (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 – MCLK divide by 2</td>
</tr>
<tr>
<td>SCLK_INV</td>
<td>5</td>
<td>0 – normal (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 – BCLK inverted</td>
</tr>
<tr>
<td>BCLKDIV</td>
<td>4:0</td>
<td>00000 – master mode BCLK generated automatically based on the clock table (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00001 – MCLK/1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00010 – MCLK/2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00011 – MCLK/3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00100 – MCLK/4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00101 – MCLK/5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00110 – MCLK/6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00111 – MCLK/7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01000 – MCLK/10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01001 – MCLK/11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01010 – MCLK/12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01011 – MCLK/13</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01100 – MCLK/22</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01101 – MCLK/24</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01110 – MCLK/25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11000 – MCLK/30</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11010 – MCLK/32</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11100 – MCLK/34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Others – MCLK/4</td>
</tr>
</tbody>
</table>

5.2 MCLK / LRCK ratio and MCLK / SCLK ratio

In master mode, the SCLK and LRCK signals are generated by ES8328E when any of the ADCs or DACs is enabled.

In slave mode, the SCLK and LRCK clock outputs are disabled by default to allow another digital audio interface to drive these pins.

ES8328E include stereo ADC and stereo DAC. The ADC and DAC have individual LRCK clock. The LRCK clock for ADC is named ALRCK. The LRCK clock for DAC is named DLRCK. Bit7(slrc) in register 43 can be used to select the same LRCK or individual LRCK for ADC and DAC. If the same LRCK is selected (slrc=1), Bit6(lrck_sel) in Register 43 can be used to select ALRCK or DLRCK as the common LRCK.
Register 0x0D is used for ADC MCLK/LRCK ratio setting. Register 0x18 is used for DAC MCLK/LRCK ratio setting. Please refer to the MCLK/LRCK table listed below.

In slave mode, ES8328E will auto-check MCLK/LRCK ratio. Only the left side ratios in the table are supported in slave mode.

In master mode, all ratios in the table are supported. Codec send the LRCK to external CPU/DSP/MCU according to MCLK / LRCK ratio setting. The value of register 0x0D and register 0x18 must be suitable for LRCK frequency.

Please refer to the diagram below to learn about the MCLK / LRCK ratio.

The BCLKDIV control bits in register 8 are used for MCLK/SCLK ratio setting. Please refer to the BCLKDIV table listed below.
In slave mode, Codec will auto-check the MCLK/SCLK ratio in slave mode. Thus BCLKDIV control bits in register 0x08 should be “00000” in slave mode.

In master mode, Codec send SCLK signal to external CPU/DSP/MCU according to MCLK/SCLK ratio setting. If the SFI of codec is I2S-24bit, the frequency of SCLK is usually equal to 64 or 48 times frequency of LRCK. If the SFI of codec is I2S-16bit, the frequency of SCLK is usually equal to 32 times frequency of LRCK.

MCLK / SCLK ratio vs. SCLK Frequency in Master mode

<table>
<thead>
<tr>
<th>Master Mode</th>
<th>Digital Audio Interface Format</th>
<th>SCLK Frequency (Minimum)</th>
<th>BCLKDIV(Maximum)</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2S</td>
<td>I2S / Left Justified / Right Justified / DSP -16bit</td>
<td>SCLK = 32 x LRCK</td>
<td></td>
</tr>
<tr>
<td>I2S</td>
<td>I2S / Left Justified / Right Justified / DSP -18bit</td>
<td>SCLK = 36 x LRCK</td>
<td></td>
</tr>
<tr>
<td>I2S</td>
<td>I2S / Left Justified / Right Justified / DSP -20bit</td>
<td>SCLK = 40 x LRCK</td>
<td></td>
</tr>
<tr>
<td>I2S</td>
<td>I2S / Left Justified / Right Justified / DSP -24bit</td>
<td>SCLK = 48 x LRCK</td>
<td></td>
</tr>
<tr>
<td>I2S</td>
<td>I2S / Left Justified / Right Justified / DSP -32bit</td>
<td>SCLK = 64 x LRCK</td>
<td></td>
</tr>
</tbody>
</table>

5.3 Four Digital Audio Formats

ES8328E supports 4 digital audio formats.

- I2S
- Left Justified
- Right Justified
- DSP Mode (PCM)

All of these four formats are MSB first.
The register 12 and register 23 are used for ADC and DAC formats.
ES8328E User Guide

I²S Serial Audio Data Format Up To 24-bit

Left Justified Serial Audio Data Format Up To 24-bit

Right Justified Serial Audio Data Format Up To 24-bit

DSP (PCM) Mode A

DSP (PCM) Mode B
6 Chip control and Power management Register

Some registers are used to ES8328E power management. These register’s address located from register 0 to register 6. The register 0 and register 1 should be used to control the internal bias current and internal reference voltage of ES8328E. The control bits in these two registers must be enabled when ES8328E start up. The register 2 should be used to control the digital block, state machine, DLL and internal reference voltage. The bits in register 2 must be zero when ES8328E start up. The register 3 should be used to power up DAC and Line inputs. The register 3 should be used to power up DAC and Line outputs. The register 5 and register 6 should be used to set low power mode.

6.1.1 Register 0 – Chip Control 1, Default 0000 0010

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCKReset</td>
<td>7 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = reset control register to default</td>
</tr>
<tr>
<td>LRCM</td>
<td>6 0 = ALRCK disabled when both ADC disabled; DLRCK disabled when both DAC disabled</td>
</tr>
<tr>
<td></td>
<td>1 = ALRCK and DLRCK disabled when all ADC and DAC disabled</td>
</tr>
<tr>
<td>DACMCLK</td>
<td>5 0 = when SameFreq, DACMCLK is the chip master clock source (default)</td>
</tr>
<tr>
<td></td>
<td>1 = when SameFreq, DACMCLK is the chip master clock source</td>
</tr>
<tr>
<td>SameFs</td>
<td>4 0 = ADC Fs differs from DAC Fs (default)</td>
</tr>
<tr>
<td></td>
<td>1 = DAC Fs is the same as DAC Fs</td>
</tr>
<tr>
<td>SeqEn</td>
<td>3 0 = internal power up/down sequence disable (default)</td>
</tr>
<tr>
<td></td>
<td>1 = internal power up/down sequence enable</td>
</tr>
<tr>
<td>EnRef</td>
<td>2 0 = disable reference</td>
</tr>
<tr>
<td></td>
<td>1 = enable reference (default)</td>
</tr>
<tr>
<td>VMIDSEL</td>
<td>1 00 = Vmid disabled</td>
</tr>
<tr>
<td></td>
<td>01 = 50 kΩ divider enabled</td>
</tr>
<tr>
<td></td>
<td>10 – 500 kΩ divider enabled (default)</td>
</tr>
<tr>
<td></td>
<td>11 = 5 kΩ divider enabled</td>
</tr>
</tbody>
</table>

6.1.2 Register 2 – Chip Power Management, Default 1100 0011

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>adc_DigDPDN</td>
<td>7 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = resets ADC DEM, filter and serial data port (default)</td>
</tr>
<tr>
<td>dac_DigDPDN</td>
<td>6 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = resets DAC DSM, DEM, filter and serial data port (default)</td>
</tr>
<tr>
<td>adc_vin_rst</td>
<td>5 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = reset ADC state machine to power down state</td>
</tr>
<tr>
<td>dac_vin_rst</td>
<td>4 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = reset DAC state machine to power down state</td>
</tr>
<tr>
<td>ACDCLL_PDN</td>
<td>3 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = ADC_PLL power down, stop ADC clock</td>
</tr>
<tr>
<td>DACDLL_PDN</td>
<td>2 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = DAC DLL power down, stop DAC clock</td>
</tr>
<tr>
<td>ad/HvRef_PDN</td>
<td>1 0 = ADC analog reference power up</td>
</tr>
<tr>
<td></td>
<td>1 = ADC analog reference power down (default)</td>
</tr>
<tr>
<td>dac/HvRef_PDN</td>
<td>0 0 = DAC analog reference power up</td>
</tr>
<tr>
<td></td>
<td>1 = DAC analog reference power down (default)</td>
</tr>
</tbody>
</table>

6.1.3 Register 3 – DAC Power Management, Default 1100 0000

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>P0nDACL</td>
<td>7 0 = left DAC power up</td>
</tr>
<tr>
<td></td>
<td>1 = left DAC power down (default)</td>
</tr>
<tr>
<td>P0nDACR</td>
<td>6 0 = right DAC power up</td>
</tr>
<tr>
<td></td>
<td>1 = right DAC power down (default)</td>
</tr>
<tr>
<td>LOUT1</td>
<td>5 0 = LOUT1 disabled (default)</td>
</tr>
<tr>
<td></td>
<td>1 = LOUT1 enabled</td>
</tr>
<tr>
<td>ROUT1</td>
<td>4 0 = ROUT1 disabled (default)</td>
</tr>
<tr>
<td></td>
<td>1 = ROUT1 enabled</td>
</tr>
<tr>
<td>LOUT2</td>
<td>3 0 = LOUT2 disabled (default)</td>
</tr>
<tr>
<td></td>
<td>1 = LOUT2 enabled</td>
</tr>
<tr>
<td>ROUT2</td>
<td>2 0 = ROUT2 disabled (default)</td>
</tr>
<tr>
<td></td>
<td>1 = ROUT2 enabled</td>
</tr>
</tbody>
</table>

6.1.4 Register 4 – Chip Power Management, Default 1111 1100

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>P0nAINL</td>
<td>7 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = left analog input power down (default)</td>
</tr>
<tr>
<td>P0nAINR</td>
<td>6 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = right analog input power down (default)</td>
</tr>
<tr>
<td>P0nADC</td>
<td>5 0 = left ADC power up</td>
</tr>
<tr>
<td></td>
<td>1 = left ADC power down (default)</td>
</tr>
<tr>
<td>P0nADCR</td>
<td>4 0 = right ADC power up</td>
</tr>
<tr>
<td></td>
<td>1 = right ADC power down (default)</td>
</tr>
<tr>
<td>P0nMIC5</td>
<td>3 0 = microphone bias power on</td>
</tr>
<tr>
<td></td>
<td>1 = microphone bias power down (high impedance output, default)</td>
</tr>
<tr>
<td>P0nADCBiasen</td>
<td>2 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = biasen power down (default)</td>
</tr>
<tr>
<td>PeakLP</td>
<td>1 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = flash ADC low power</td>
</tr>
<tr>
<td>IntLP</td>
<td>0 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = low power</td>
</tr>
</tbody>
</table>

6.1.5 Register 5 – Chip Low Power 1, Default 0000 0000

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPACCL</td>
<td>7 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = low power</td>
</tr>
<tr>
<td>LPACCR</td>
<td>6 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = low power</td>
</tr>
<tr>
<td>LPLOUT1</td>
<td>5 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = low power</td>
</tr>
<tr>
<td>LPLOUT2</td>
<td>3 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = low power</td>
</tr>
</tbody>
</table>

6.1.6 Register 6 – Chip Low Power 2, Default 0000 0000

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPPODA</td>
<td>7 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = low power</td>
</tr>
<tr>
<td>LPMIX</td>
<td>8 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = low power</td>
</tr>
<tr>
<td>LPADcR</td>
<td>1 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = low power</td>
</tr>
<tr>
<td>LPADcR0</td>
<td>0 0 = normal</td>
</tr>
<tr>
<td></td>
<td>1 = low power</td>
</tr>
</tbody>
</table>
7 Analog input signal path

ES8328E has 4 analog input pins which may be used to support connections to multiple microphone or line input sources. The input multiplexers on the left and right channels can be used to select different configurations for each of the input sources. The analog input paths can support line inputs or microphone inputs, in single-ended mode, pseudo-differential and fully-differential modes. The input stage can also provide common mode noise rejection in some configurations.

The Left and Right analog input channels are routed to ADCs where it is digitised. Alternatively, the two channels can also be mixed in the analog domain and digitized in one ADC while the other ADC is switch off. The mono-mix signal appears on both digital output channels.

There is also a BYPASS path for each channel, enabling the analog input signal to be routed directly to the output multiplexers and PGAs.

7.1 The Analog input signal paths and the control register

The ES8328E analog input signal paths and control registers are illustrated in the figure which be listed below.

pdnAINL and pdnAINR control bits in register 3 should be used to power up / power down the input channel.

In this figure, LINSSEL and RINSSEL control bits are used to select independently between external inputs and internally generated differential products (LIN1-RIN1 or LIN2-RIN2). The choice of differential signal, LIN1-RIN1 or LIN2-RIN2 is made using DS, DSSEL and DSR control bits.

Example 1, the ES8328E can be set up to convert one differential signal by applying the differential signal to LIN1/RIN1. By setting the LINSSEL and RINSSEL to L-R differential and setting the DSSEL, DSR and DS to zero, the differential signal can then be routed to the Left/Right ADCs.

Example 2, the ES8328E can be set up to convert two differential signal by applying one differential signal to LIN1/RIN1 and applying the other to LIN2/RIN2. By setting the LINSSEL and RINSSEL to L-R differential, setting the DSSEL and DSR to one and setting DS to zero, the LIN1/RIN1 differential signal can be routed to the Left ADC and the LIN2/RIN2 differential signal can be routed to Right ADC.

MicAmpL and MicAmpR control bits are used to control PGA to amplify the amplitude of input signals. The input signals are selected by LINSSEL and RINSSEL control bits. The PGA gain is adjustable from 0dB to +24dB in 3dB steps.

The two input channels can also be mixed in the analog domain and digitized in one ADC while the other ADC is switch off. By setting MONOMIX to '01' or '10', the mono-mix signal can then be routed to Left ADC or Right ADC. For analog mono mix either the left or right ADC can be used, allowing the unused ADC to be powered off. The user also has the flexibility to select the data output from the audio interface using DATSEL control bits.

LMIXSEL and RMIXSEL control bits are used to select the input channel of Left and Right Bypass path. The selected input channels can be routed directly to the the output multiplexers and PGAs.
7.2 Single-ended Microphone input

ES8328E should be used in single-ended microphone input mode when LINSEL and RINSEL in Register 10 don’t be set to ‘11’. The single-ended microphone input signal can be connected to LIN1, RIN1, LIN2 or RIN2. The MicAmpL or MicAmpR can be used to boost the microphone signal level.

Single-ended microphone mode can not provide common mode noise rejection.
7.3 Pseudo-differential Microphone input

ES8328E should be used in pseudo-differential microphone input mode when LINSEL and RINSEL in Register 10 are set to '11'. The pseudo-differential microphone input signal can be connected to LIN1 and RIN1 or LIN2 and RIN2. The MicAmpL and MicAmpR can be used to boost the microphone signal level. When GND has obvious noise, Pseudo-differential microphone mode can provide common mode noise rejection.

7.4 Fully-differential Microphone input

ES8328E should be used in fully-differential microphone input mode when LINSEL and RINSEL in Register 10 are set to '11'. The fully-differential microphone input signal can be connected to LIN1 and RIN1 or LIN2 and RIN2. The MicAmpL and MicAmpR can be used to boost the microphone signal level. Fully-differential microphone mode can provide common mode noise rejection. The recording volume in fully-differential mode should be 2 times volume of pseudo-differential mode.

The fully-differential microphone mode is recommended for microphone recording.

8 ADC For Recording

ES8328E can provide a stereo ADC for recording via I2S/PCM interface. The digital output data is sent out on ASDOUT pin. The ADC full scale input level is proportional to AVDD. With a 3.3V supply voltage, the full scale level is 1.0Vrms. Any voltage greater than full scale may overload the ADC and cause distortion.

One ALC module should be used for recording. The registers used for ALC is located from register 18 to register 22.
8.1 The ADC block diagram

8.2 The ADC Control Registers

PdnADCL and PdnADCR control bits in register 3 should be used to power up / power down Left and right ADC. ADC_invL control bit in register 14 are used to invert the polarity of left channel ADC. ADC_invR control bit in register 14 are used for right channel ADC.

ADC_HPF_L and ADC_HPF_R control bits in register 14 are used to enable or disable high pass filter of left and right channel ADC. The default setting are recommended to ADC_HPF_L and ADC_HPF_R.

ADCSofRamp control bit is used to fade in and fade out. ADRampRate control bits are used to set the soft ramp rate.

ES8328E ADC’s digital volume can be adjustable from -96dB to 0dB in 0.5dB steps. LADCVOl and RADCVOl is used to independently control the left an right ADC recording volume. If ADCLeR control bit in register 15 is set to ‘1’, the volume of left and right ADC can adjust synchronously by adjusting left ADC volume.

ES8328E ADC should be mute by setting ADCMute to ‘1’.

---

**8.1 The ADC block diagram**

**8.2 The ADC Control Registers**

PdnADCL and PdnADCR control bits in register 3 should be used to power up / power down Left and right ADC.

ADC_invL control bit in register 14 are used to invert the polarity of left channel ADC. ADC_invR control bit in register 14 are used for right channel ADC.

ADC_HPF_L and ADC_HPF_R control bits in register 14 are used to enable or disable high pass filter of left and right channel ADC. The default setting are recommended to ADC_HPF_L and ADC_HPF_R.

ADCSofRamp control bit is used to fade in and fade out. ADRampRate control bits are used to set the soft ramp rate.

ES8328E ADC’s digital volume can be adjustable from -96dB to 0dB in 0.5dB steps. LADCVOl and RADCVOl is used to independently control the left an right ADC recording volume. If ADCLeR control bit in register 15 is set to ‘1’, the volume of left and right ADC can adjust synchronously by adjusting left ADC volume.

ES8328E ADC should be mute by setting ADCMute to ‘1’.

---

**6.1.4 Register 3 – ADC Power Management, Default 1111 1100**

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PdnADCL</td>
<td>5</td>
<td>0 – left ADC power up 1 – left ADC power down (default)</td>
</tr>
<tr>
<td>PdnADCR</td>
<td>4</td>
<td>0 – right ADC power up 1 – right ADC power down (default)</td>
</tr>
</tbody>
</table>

**6.2.6 Register 14 – ADC Control 8, Default 0011 0000**

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC_invL</td>
<td>7</td>
<td>0 – normal (default) 1 – left channel polarity inverted</td>
</tr>
<tr>
<td>ADC_invR</td>
<td>6</td>
<td>0 – normal (default) 1 – right channel polarity inverted</td>
</tr>
<tr>
<td>ADC_HPF_L</td>
<td>5</td>
<td>0 – disable ADC left channel high pass filter 1 – enable ADC left channel high pass filter (default)</td>
</tr>
<tr>
<td>ADC_HPF_R</td>
<td>4</td>
<td>0 – disable ADC right channel high pass filter 1 – enable ADC right channel high pass filter (default)</td>
</tr>
</tbody>
</table>

**6.2.7 Register 15 – ADC Control 7, Default 0011 0000**

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADCRampRate</td>
<td>7:6</td>
<td>0 – 0.5 dB per 4 LRCK digital volume control ramp rate (default) 01 – 0.5 dB per 8 LRCK digital volume control ramp rate 10 – 0.5 dB per 16 LRCK digital volume control ramp rate 11 – 0.5 dB per 32 LRCK digital volume control ramp rate</td>
</tr>
<tr>
<td>ADCSoftRamp</td>
<td>5</td>
<td>0 – disabled digital volume control soft ramp 1 – enabled digital volume control soft ramp (default)</td>
</tr>
<tr>
<td>ADCLeR</td>
<td>3</td>
<td>0 – normal (default) 1 – both channel gain control is set by ADC left gain control register</td>
</tr>
<tr>
<td>ADCMute</td>
<td>2</td>
<td>0 – normal (default) 1 – mute ADC digital output</td>
</tr>
</tbody>
</table>

**6.2.8 Register 16 – ADC Control 9, Default 1100 0000**

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LADCVOl</td>
<td>7:0</td>
<td>Digital volume control attenuates the signal in 0.5 dB incremental from 0 to -96 dB. 00000000 – 0 dB 00000001 – 0.5 dB 00000010 – 1 dB ... 11000000 – -96 dB (default)</td>
</tr>
</tbody>
</table>

**6.2.9 Register 17 – ADC Control 9, Default 1100 0000**

<table>
<thead>
<tr>
<th>Bit Name</th>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RADCVOl</td>
<td>7:0</td>
<td>Digital volume control attenuates the signal in 0.5 dB incremental from 0 to -96 dB. 00000000 – 0 dB 00000001 – 0.5 dB 00000010 – 1 dB ... 11000000 – -96 dB (default)</td>
</tr>
</tbody>
</table>
8.3 Automatic Level Control (ALC)

In applications that offer a recording feature, ALC is often desirable to keep the recorded signal at a constant level. For example, if recording voice, the signal may vary a great deal depending on how loud the user speaks or how close to the mouth the microphone is held. This will result in a recorded signal that is difficult to listen to when played back.

The purpose of the ALC is to keep a constant output volume irrespective of the input signal level. This is achieved by continually adjusting the PGA gain so that the signal level at the ADC output remains constant.

Setting up the ALC to be optimal for each recorded source such as voice, classical music, pop music, etc. is quite a complex process. Recommended setups have been provided as a base to work from. The resultant effect is very subjective and may vary between applications. Some further modifications may be required to optimize the feature for a specific application but the recommended settings should offer suitable solutions in most cases.

There are some registers which can be used to control ALC. Please refer to the register list below.

<table>
<thead>
<tr>
<th></th>
<th></th>
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<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Reg. 18</td>
<td>ALC Control 1</td>
<td>ALCSEL</td>
<td>MAXGAIN</td>
<td>MINGAIN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0011 1000</td>
</tr>
<tr>
<td>Reg. 19</td>
<td>ALC Control 2</td>
<td></td>
<td>ALCSEL</td>
<td></td>
<td>ALCSLE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1011 0000</td>
</tr>
<tr>
<td>Reg. 20</td>
<td>ALC Control 3</td>
<td>ALCSEL</td>
<td></td>
<td>ALCSLE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0011 0010</td>
</tr>
<tr>
<td>Reg. 21</td>
<td>ALC Control 4</td>
<td>ALCSEL</td>
<td>ALCCNC</td>
<td>TIME_OUT</td>
<td></td>
<td>WIN_SIZE</td>
<td></td>
<td></td>
<td></td>
<td>0000 0110</td>
</tr>
<tr>
<td>Reg. 22</td>
<td>ALC Control 5</td>
<td></td>
<td>ALCMODE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0000 0000</td>
</tr>
</tbody>
</table>

8.3.1 CONTROL FIELDS

The ALC function in ES8328E CODEC is highly adaptable on account of the number of different parameters that may be individually set. The following paragraphs describe each of these parameters, and also some of the constraints or tradeoffs that determine the optimum setting for each. Different parameter values will be desirable to suit different types of audio signal. Personal preferences can also influence the choice of settings.

**ALC Enable / ALC Level.** The ALC function is enabled by setting the register field ALCSEL. ALCSEL=2'b00: ALC OFF; ALCSEL=2'b01: ALC Right Channel Enabled; ALCSEL=2'b10: ALC Left Channel Enabled; ALCSEL=2'b11: ALC Enabled. When enabled, the ALC output volume can be programmed using the ALCVL register field. The range of ALC Level varies between 0dBFS and -16.5dBFS with 1.5dBFS per step.

The maximum target level is always not above ADC full-scale level to help reduce the possibility of clipped signals. This level should be set as high as possible in order to achieve the best signal to noise performance, but not so high as to allow signal clipping to occur as the signal changes. The more erratic the signal level, the greater the required headroom between the ALC Target Level and the ADC full-scale level.

**ALC Maximum Gain.** An upper limit for the PGA gain is imposed by setting the register field MAXGAIN. The range of MAXGAIN varies between -6.5dBFS and 35.5dBFS with 6dBFS per step. The purpose of the maximum gain is to ensure the small input signals are accommodated and not excessively amplified by the ALC function. For example, if a recorded music track fades out; the Maximum Gain setting prevents ALC from destroying the effect by continually increasing the gain as the music signal fades.

The Maximum Gain setting prevents ALC from being driven out by the signal level of the ADC full-scale level.

**ALC Minimum Gain.** A lower limit for the PGA gain is imposed by setting the register field MINGAIN. The range of MINGAIN varies between -12dBFS and 30dBFS with 6dBFS per step. The purpose of the minimum gain is to ensure that large input signals are permitted and not excessively attenuated by the ALC function. If the Minimum Gain is large, then the ALC will be restricted in its ability to control the signal level and there is a greater possibility that it will be unable to prevent distortion of large signals. However, if the Minimum Gain is small, then a greater attenuation will be applied to large signals, which may undesirably limit the dynamic range of the processed signal. The Minimum Gain should be set as low as is possible, and certainly no greater than the gain that would be required to adjust the largest input signal down to the

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ES8328E User Guide 2011-06-17
8.3.2 Recommended Settings for ALC

Recommended settings are provided below for a number of typical portable recording applications. These include voice recording and music recording. A generic setting is also provided, which aims to cater for the widest possible range of sounds.

It is important to note that these are suggested initial values only, as a starting point from which to derive the best settings for a particular circuit application. The quoted settings should give adequate performance in many cases, but it may be possible to improve the ALC performance through further adjustment of these settings.
For voice recording, a fast ALC response is desirable in order to quickly compensate for different peoples voices, movement relative to the microphone.

For music recording, the fast response is not recommended as it is likely to result in clipping in response to any sudden changes in the music signal level. A reduction in the maximum gain setting may help to avoid clipping when the music level increases after a quiet period and to restrict the extent of the ALC adjustments. This may not be desirable in all music applications and is therefore not shown in the recommended settings. It is one of the many adjustments that the user should consider when optimizing for a known operational environment.

For generic recording, the ALC must attempt to accommodate all types of sounds, a compromise setting must be found. For an ALC response that is tolerant to impulses such as handclaps, it is recommended that the ALC Attack time should not be set too fast and the ALC Decay time should not be set too slow. The minimum and maximum gain settings could be adjusted to restrict the extent of the ALC control if desired. The combination of settings should allow the ALC to respond quickly to changes in signal level and to impulse-type sounds, but also to minimize gain pumping caused by the associated level changes.

The settings in following table are the recommended settings for voice, music and generic (hand clap).

<table>
<thead>
<tr>
<th>REGISTER BIT</th>
<th>RECOMMENDED VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALCSEL[1:0]</td>
<td>11 (Stereo)</td>
</tr>
<tr>
<td>ALCCLVL[3:0]</td>
<td>1100 (-4.5dB)</td>
</tr>
<tr>
<td>MAXGAIN[2:0]</td>
<td>101 (+23.5dB)</td>
</tr>
<tr>
<td>MINGAIN[2:0]</td>
<td>010 (0dB)</td>
</tr>
<tr>
<td>ALCNLD[3:0]</td>
<td>0000 (0ms)</td>
</tr>
<tr>
<td>ALCDCY[3:0]</td>
<td>0001 (820us/step)</td>
</tr>
<tr>
<td>ALCATK[3:0]</td>
<td>0010 (416us/step)</td>
</tr>
<tr>
<td>ALCMODE</td>
<td>0 (ALC)</td>
</tr>
<tr>
<td>ALCZC</td>
<td>0 (ZC off)</td>
</tr>
<tr>
<td>TIME_OUT</td>
<td>0 (not enable)</td>
</tr>
<tr>
<td>NGTH[4:0]</td>
<td>11000 (-40.5dB)</td>
</tr>
<tr>
<td>NGQ[1:0]</td>
<td>01 (mule ADC)</td>
</tr>
<tr>
<td>WIN_SIZE[4:0]</td>
<td>0x077 (+21dB)</td>
</tr>
</tbody>
</table>

8.4 Microphone input circuit and the sample code for recording

In recording mode, the analog input pins can be used as single ended input or differential input. Some microphone input circuits (single ended input or differential input) and sample code for recording are listed below. In microphone recording mode, ALC should be enabled to boost the microphone input signal.

Please note that the fully-differential input circuit and pseudo-differential input circuit are recommended to ES8328E microphone recording.

8.4.1 Fully-Differential Microphone input circuit and sample code
Notes:
1. On PCB layout, these wires which be marked as red must be paralleled each other.
2. On PCB layout, the components such as R1, R2, R3, C1, C2, C3, C4, C5 and C6 must be located as close to Microphone as possible.

The sample code for microphone differential input:
```
ES8328E_write(0x02, 0xF3);  // Reg0x02 = 0xF3, Stop STM, DLL, and digital block
ES8328E_write(0x08, 0x00);  // Reg 0x08 = 0x00, ES8328E in I2S slave mode
//ES8328E_write(0x08, 0x80);  // Reg 0x08 = 0x80 (ES8328E in I2S master mode)
ES8328E_write(0x2B, 0x80);  // Reg 0x2B = 0x80 (Set ADC and DAC have the same LRCK)
ES8328E_write(0x00, 0x05);  // Reg 0x00 = 0x05 (start up reference)
ES8328E_write(0x01, 0x40);  // Reg 0x01 = 0x40 (start up reference)
ES8328E_write(0x03, 0x00);  // Reg 0x03 = 0x00 (Power on ADC and LIN/RIN input)
ES8328E_write(0x09, 0x77);  // Reg 0x09 = 0x77 (MicBoost PGA=+21Db)
ES8328E_write(0x0A, 0xF0);  // Reg 0x0A = 0xF0 (differential input)
ES8328E_write(0x0B, 0x02);  // Reg 0x0B = 0x02 (Select LIN1 and RIN1 as differential input pairs)
// ES8328E_write(0x0B, 0x82);  // Reg 0x0B = 0x82 (Select LIN2 and RIN2 as differential input pairs)
ES8328E_write(0x0C, 0x40);  // Reg 0x0C = 0x40 (I2S – 24bits, Ldata = LADC, Rdata = RADC)
ES8328E_write(0x0D, 0x02);  // Reg 0x0D = 0x02 (MCLK/LRCK = 256)
ES8328E_write(0x00, 0x05);  // Reg 0x00 = 0x05 (start up reference)
ES8328E_write(0x01, 0x40);  // Reg 0x01 = 0x40 (start up reference)
ES8328E_write(0x03, 0x00);  // Reg 0x03 = 0x00 (Power on ADC and LIN/RIN input)
ES8328E_write(0x09, 0x77);  // Reg 0x09 = 0x77 (MicBoost PGA=+21Db)
```

8.4.2 Pseudo-Differential Microphone input circuit and sample code

Notes:
1. On PCB layout, these wires which be marked as red must be paralleled each other.
2. On PCB layout, the components such as R4, R5, C7, C8, C9, C10, and C11 must be located as close to Microphone as possible.

The sample code for microphone pseudo differential input:
```
ES8328E_write(0x02, 0xF3);  // Reg0x02 = 0xF3, Stop STM, DLL, and digital block
ES8328E_write(0x08, 0x00);  // Reg 0x08 = 0x00, ES8328E in I2S slave mode
//ES8328E_write(0x08, 0x80);  // Reg 0x08 = 0x80 (ES8328E in I2S master mode)
ES8328E_write(0x2B, 0x80);  // Reg 0x2B = 0x80 (Set ADC and DAC have the same LRCK)
ES8328E_write(0x00, 0x05);  // Reg 0x00 = 0x05 (start up reference)
ES8328E_write(0x01, 0x40);  // Reg 0x01 = 0x40 (start up reference)
ES8328E_write(0x03, 0x00);  // Reg 0x03 = 0x00 (Power on ADC and LIN/RIN input)
ES8328E_write(0x09, 0x77);  // Reg 0x09 = 0x77 (MicBoost PGA=+21Db)
```
8.4.3 Single ended Microphone input circuit and sample code

Notes:
1. On PCB layout, the components such as R6, R7, C12, C13, C14, and C15 must be located as close to Microphone as possible.

2. In customer application, the microphone single ended input circuit must not be recommended for ES8328 microphone recording.

The sample code for microphone single ended input:

```
ES8328E_write(0x02, 0xF3);  // Reg0x02 = 0xF3, Stop STM, DLL, and digital block
ES8328E_write(0x08, 0x00);   // Reg 0x08 = 0x00, ES8328E in I2S slave mode
//ES8328E_write( 0x08 0x80);  // Reg 0x08 = 0x80 (ES8328E in I2S master mode)
ES8328E_write(0x2B, 0x80);  // Reg 0x2B = 0x80 (Set ADC and DAC have the same LRCK)
ES8328E_write(0x00, 0x05);  // Reg 0x00 = 0x05 (start up reference)
ES8328E_write(0x01, 0x40);  // Reg 0x01 = 0x40 (start up reference)
ES8328E_write(0x03, 0x00);  // Reg 0x03 = 0x00 (Power on ADC and LIN/RIN input)
ES8328E_write(0x09, 0x77);  // Reg 0x09 = 0x77 (MicBoost PGA=+21Db)
ES8328E_write(0xA0, 0x00);  // Reg 0xA0 = 0xF0 (Lin1 and RIN1 used as single ended input)
//ES8328E_write( 0xA0 0x50);  // Reg 0xA0 = 0xF0 (Lin2 and RIN2 used as single ended input)
ES8328E_write(0xC0, 0x40);  // Reg 0x0C = 0x00 (I2S – 24bits, Ldata = LADC, Rdata = RADC)
ES8328E_write(0xD0, 0x02);  // Reg 0xD0 = 0x02 (MCLK/LRCK = 256)
ES8328E_write(0x10, 0x00);  // Reg 0x10= 0x00 (LADC volume = 0dB)
ES8328E_write(0x11, 0x00);  // Reg 0x11= 0x00 (RADC volume = 0dB)
ES8328E_write(0x12, 0xe2);  // Reg 0x12 = 0xe2 (ALC enable, PGA Max. Gain=23.5dB, Min. Gain=0dB)
ES8328E_write(0x13, 0xa0);  // Reg 0x13 = 0xc0 (ALC Target=-4.5dB, ALC Hold time =0 mS)
ES8328E_write(0x14, 0x12);  // Reg 0x14 = 0x12 (Decay time =820uS , Attack time = 416 uS)
ES8328E_write(0x15, 0x06);  // Reg 0x15 = 0x06(ADC mode)
ES8328E_write(0x16, 0xc3);  // Reg 0x16 = 0xc3 (nose gate = -40.5dB, NGG = 0x01(mute ADC))
ES8328E_write(0x02, 0x55);  // Reg 0x16 = 0x55 (Start up DLL, STM and Digital block for recording)
```
9 Output Signal Path

ES8328E output signal path consist of digital filters, DACs, Analog mixers and Output drivers. The digital filters and DACs are enabled when ES8328E is in ‘play back mode’ or ‘record and play back mode’. The mixers and output drivers can be separately enabled by individual control bits. Thus it is possible to utilize the analog mixing and amplification provided by ES8328E, irrespective of whether the DACs are running or not.

ES8328E receives digital input data on DSDIN pin. The digital filter block process the data to provide the following functions:
- Digital volume control
- Equalizer and stereo enhancement
- Sigma-Delta Modulation

Two high performance sigma-delta audio DACs convert the digital input data into two analog signals (left and right). These can be mixed with analog input signals from LIN1/2 and RIN1/2 pins, and the mixed is fed to the output drivers, LOUT1/ROUT1 and LOUT2/ROUT2.
- LOUT1/ROUT1: can drive 16Ω or 32Ω stereo headphone or stereo line output
- LOUT2/ROUT2: can drive 16Ω or 32Ω stereo headphone or stereo line output

9.1 The Output Signal Paths And The Control Register

PdnDACL and PdnDACR control bits in register 4 are used to power up / power down Left and Right channel DAC.
LOUT1, ROUT1, LOUT2 and ROUT2 control bits in register 4 are used to power up / power down output drivers, LOUT1, ROUT1, LOUT2 and ROUT2.

The signal volume on LOUT1, ROUT1, LOUT2 and ROUT2 can be independently adjusted under software control by writing LOUT1VOL, ROUT1VOL, LOUT2VOL and ROUT2VOL, respectively. The output driver volume is adjustable from -45dB to +4.5dB in 1.5dB steps. Note that the volume over 0dB may cause clipping if signal is large.

Left and right mixers are used to mix the DAC’s output and the analog input signal which be selected by LMIXSEL and RMIXSEL. If L2LO control bits in register 39 is set to ‘1’, the analog input signal which be selected by LMIXSEL should be mixed in left mixer. If R2RO control bits in register 42 is set to ‘1’, the analog input signal which be selected by RMIXSEL should be mixed in right mixer.

The mixed signal can be controlled with Mixer PGAs (L2LOVOL and R2ROVOL). The gain of Mixer PGA is adjustable from -15dB to +6dB in 3dB steps. The left mixed is fed to LOUT1 and LOUT2 output drivers, and the right mixed is fed to ROUT1 and ROUT2 output drivers.
### 9.2 The DAC Control Register

PdnDACL and PdnDACR control bits in register 4 are used to power up / power down Left and Right channel DAC. Please refer to section 9.2.

ES8328E DAC’s digital volume can be adjustable from -96dB to 0dB in 0.5dB steps. LDACVOL and RDACVOL is used to independently control the left an right DAC volume. If DACLeR control bit in register 25 is set to ’1’, the volume of left and right DAC can adjust synchronously by adjusting left DAC volume. DACs should be mute if DACMute control bit in register 25 is set to ’1’.

ZeroL and ZeroR control bits in register 29 are used to set the left and right channel DACs output all zero. This operation is equivalent to mute the DAC or set the DAC digital volume to -96dB.

DAC_invL control bit in register 28 are used to invert the left channel DAC output, and DAC_invR control bit in register 28 is used for right channel DAC.

DACSoft Ramp control bit in register 25 is use to fade in and fade out. DACRampRate control bits are used to set the soft ramp rate.

Mono control bit is used to set the DAC in stereo output mode or mono output mode.
9.3 Equalizer and Stereo Enhancement

ES8328E provides equalizer and stereo enhancement function in play back mode. These cannot be used in Bypass mode.

For equalizer, only 2 band equalizer is used. It can do bass or treble operation, but cannot do bass and treble operation at the same time. Everest Semiconductor Co., Ltd will provide equalizer calculator to help user to utilize this equalizer.

The equalizer register address is located from register 30 to register 37.

The SE control bits in register 29 are used to set the stereo strength. There are 8 levels stereo strength from 0 to 7. ES8328E will get the strongest stereo effect if SE equal to 7. There is not any stereo enhancement if SE equal to 0.

10 Register Configuration Sequence for ES8328E

The Register configuration sequence include start up codec mode, start up recording mode, start up play back mode, start up pass mode, power down (to standby mode), resume from standby mode, etc.
10.1 The Sequence for Start up codec

Start

Set Chip to Master / Slave Mode
Reg 0x08 = 0x00 (Slave Mode)

Power up ADC / Analog Input / Micbias for Record
Reg 0x03 = 0x00

Select Analog input channel for ADC
Reg 0x0A = 0x00 (Lin1/Rin1)

Select Analog Input PGA Gain for ADC
Reg 0x09 = 0x00 (0dB)

Select MCLK / LRCK ratio for ADC
Reg 0x0D = 0x02 (256)

Set ADC Digital Volume
Reg 0x10 = 0x00 (0dB)
Reg 0x11 = 0x00 (0dB)

Select ALC for ADC Record
Reg 0x12 to Reg 0x16
Refer to ALC description

Power up DAC and Enable LOUT/ROUT
Reg 0x04 = 0x3C

Set ADC SFI
Reg 0x0C = 0x00 (I2S, 24BIT)

Power down DEM and STM
Reg 0x02 = 0x00

Set Chip to Play & Record Mode
Reg 0x00 = 0x05

Set DAC Digital Volume
Reg 0x1A = 0x00 (0dB)
Reg 0x1B = 0x00 (0dB)

Power up Analog and Ibias
Reg 0x01 = 0x40

Power up DAC and Enable LOUT/ROUT
Reg 0x04 = 0x3C

Select SFI for DAC
Reg 0x17 = 0x00 (I2S 24BIT)

Select MCLK / LRCK ratio for DAC
Reg 0x18 = 0x02 (256)

Setup Mixer
Reg 0x26 = 0x00
Reg 0x27 = 0xB8
Reg 0x28 = 0x38
Reg 0x29 = 0x38
Reg 0x2A = 0xB8
Please refer to Mixer description

Please refer to MCLK/LRCK ratio description

Power up DEM and STM
Reg 0x02 = 0x00

End

Only for ADC

The above item must be done step by step.

10.2 The sequence for Start up recording

Start

Set Chip to Master / Slave Mode
Reg 0x08 = 0x00 (Slave Mode)
Reg 0x08 = 0x80 (Master Mode)

Power up ADC / Analog Input / Micbias for Record
Reg 0x03 = 0x00

Select Analog input channel for ADC
Reg 0x0A = 0x00 (Lin1/Rin1)

Select Analog Input PGA Gain for ADC
Reg 0x09 = 0x88 (24dB)

Select MCLK / LRCK ratio for ADC
Reg 0x0D = 0x02 (256)

Set ADC Digital Volume
Reg 0x10 = 0x00 (0dB)
Reg 0x11 = 0x00 (0dB)

Select ALC for ADC Record
Reg 0x12 to Reg 0x16
Refer to ALC description

Power up DEM and STM
Reg 0x02 = 0x00

Set ADC SFI
Reg 0x0C = 0x00 (I2S, 24BIT)

Set MCLK / LRCK ratio for ADC
Reg 0x0D = 0x02 (256)

Set DAC Digital Volume
Reg 0x1A = 0x00 (0dB)
Reg 0x1B = 0x00 (0dB)

UnMute ADC
Reg 0x0F = 0x30 (ADC unmute)

Power up DEM and STM
Reg 0x02 = 0x55

End

Only for DAC

These will be done step by step.
10.3 The sequence for Start up play back mode

Start

Set Chip to Master / Slave Mode
Reg 0x08 = 0x00 (Slave Mode)
Reg 0x08 = 0x80 (Master Mode)

Power down DEM and STM
Reg 0x02 = 0xF3

Set same LRCK
Reg 0x2B = 0x80

Set Chip to Play & Record Mode
Reg 0x00 = 0x05

Power Up Analog and Ibias
Reg 0x01 = 0x40

Power up DAC / Analog Output for Record
Reg 0x04 = 0x3C

Set ADC Digital Volume
Reg 0x1A = 0x00 (0dB)
Reg 0x1B = 0x00 (0dB)

UnMute DAC
Reg 0x19 = 0x32 (DAC unmute)

Power up DEM and STM
Reg 0x02 = 0xAA

Set Mixer for DAC Output
Refer to Mixer description
Reg 0x26 = 0x60
Reg 0x27 = 0x88 (LDAC to Lout)
Reg 0x28 = 0x38
Reg 0x29 = 0x38
Reg 0x2A = 0x88 (RDAC to Rout)
Please refer to Mixer description

Set ADC Volume
Reg 0x2E = 0x1E (0dB)
Reg 0x2F = 0x1E (0dB)
Reg 0x30 = 0x1E (0dB)
Reg 0x31 = 0x1E (0dB)

Set Lout / Rout Volume
Reg 0x2B = 0x80

Power up DEM and STM
Reg 0x02 = 0xAA

End

These will be done step by step.

10.4 The sequence for Start up bypass mode

Start

Set Chip to Master / Slave Mode
Reg 0x08 = 0x00 (Slave Mode)
Reg 0x08 = 0x80 (Master Mode)

Power down DEM and STM
Reg 0x02 = 0xF3

Set same LRCK
Reg 0x2B = 0x80

Set Chip to Play & Record Mode
Reg 0x00 = 0x05

Power Up Analog and Ibias
Reg 0x01 = 0x40

Power down DAC, Power up Analog Input for Bypass
Reg 0x03 = 0x3F

Power down DAC, Power up Analog Output for Bypass
Reg 0x04 = 0xF0

Set Mixer for Bypass Output
Refer to Mixer description
Reg 0x26 = 0x60 (L1IN / L1OUT)
Reg 0x27 = 0x50 (LIN to LOUT)
Reg 0x28 = 0x38
Reg 0x29 = 0x38
Reg 0x2A = 0x50 (RIN to ROUT)
Please refer to Mixer description

Set Lout / Rout Volume
Reg 0x2E = 0x1E (0dB)
Reg 0x2F = 0x1E (0dB)
Reg 0x30 = 0x1E (0dB)
Reg 0x31 = 0x1E (0dB)

Power up DEM and STM
Reg 0x02 = 0xFA

Power up reference voltage
Reg 0x02 = 0xF0 or 0x00

End

These will be done step by step.
10.5  Power Down Sequence (To Standby Mode)

Start

Mute ADC and DAC
Reg 0x0F = 0x34 (ADC Mute)
Reg 0x19 = 0x36 (DAC Mute)

Power down DEM and STM
Reg 0x02 = 0xF3

Power Down ADC / Analog Input / Micbias for Record
Reg 0x03 = 0xFC

Power down DAC and disable LOUT/ROUT
Reg 0x04 = 0xC0

End

The above item must be done step by step.

10.6  Resume from standby mode Sequence

Start

Power up ADC / Analog Input / Micbias for Record
Reg 0x03 = 0x00

Power up DAC and enable LOUT/ROUT
Reg 0x04 = 0x3C

UnMute ADC and DAC
Reg 0x0F = 0x30 (ADC unmute)
Reg 0x19 = 0x32 (DAC unmute)

Power up DEM and STM
Reg 0x02 = 0x00

End

The above item must be done step by step.