Genesys Logic, Inc.

GL852GC

USB 2.0 MTT Hub Controller

Datasheet

Revision 1.09
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Revision History

Revision	Date	Description
1.00	01/28/2010	First formal release
1.01	02/11/2010	Modify 5.2.7, p.23 Modify 5.2.8, p.23
1.02	11/17/2010	Add information about DCP support, p.8, 9, 27
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1.07	07/15/2011	Update Table 3.1, 3.2, 3.3, 3.4 RREF I/O type, p.13, 14
1.08	12/22/2011	Updated Table 7.2 Operating Ranges, p. 27
1.09	02/09/2012	Support Battery Charging rev. 1.2 Updated Table 7.3 R_{DN}/R_{UP} data, p.28

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CHAPTER 1 GENERAL DESCRIPTION

GL852GC is Genesys Logic's premium 4-port hub solution which fully complies with Universal Serial Bus Specification Revision 2.0. GL852GC implements multiple TT* *(Note1)* architecture that provide dedicated TT* to each downstream (DS) ports, which guarantee Full-Speed(FS) data passing bandwidth when multiple FS device perform heavy loading operations. The controller inherits Genesys Logic's cutting edge technology on cost and power efficient serial interface design. GL852GC has proven compatibility, lower power consumption figure and better cost structure above all USB 2.0 hub solutions worldwide.

GL852GC implements multiple hub configuration features onto internal mask ROM, which traditionally requires one external EEPROM. The microprocessor detects general purpose I/O (GPIO) status during the initial stage to configure hub settings such as (1) number of DSport, (2) declare of compound device (3) gang/individual mode selection…etc. External EEPROM can be removed if no vendor specified PID/VID or product string is required for the application.

GL852GC also complies with USB-IF battery charging specification rev1.2, which can support fast charging function, allowing portable device can draw up to 1.5A from GL852GC charging downstream ports (CDP[1]) or dedicated charging port (DCP[2]).

GL852GC supports three package types, summarized as below table. LQFP48 package provides full hub features such as (1) two-color (green/amber) status LEDs for each DS ports, (2) Individual/Gang mode power management scheme that indicates DS port over-current events. (3) Number of DS ports setting configured by GPIO setting (4) non-removable declaration configured by GPIO setting (5) Support both 93C46 and 24C02 EEPROM (6) power switch polarity selections…etc. QFN28/SSOP28 package support only partial hub features but provide smaller footprint that targets space limited PCB layout environments such as embedded system or UMPC/MID applications.

Package Type	# of DS Ports	Port # Config.	Non-removable Declaration	Power Mgmt.	# of CDP/DCP Support	LED Support	EEPROM
LQFP 48	4	GPIO	EEPROM/ GPIO	Individual/Gang	4	Green/Amber	93C46/ 24C02
QFN 28	4	EEPROM	EEPROM	Individual/Gang	4	N/A	24C02
SSOP 28	4	EEPROM	EEPROM	Gang	4	N/A	24C02

GL852GC Package – Feature Summary

*Note: TT (transaction translator) is the main traffic control engine in an USB 2.0 hub to handle the unbalanced traffic speed between the upstream port and the downstream ports.

[1] CDP, charging downstream port, the Battery Charging Rev.1.2-compliant USB port that does data communication and charges device up to 1.5A.
[2] DCP, dedicated charging port, the Battery Charging Rev.1.2-compliant USB port that only charges devices up to 1.5A, similar to wall chargers.

CHAPTER 2 FEATURES

- Compliant with USB specification revision 2.0
  - Configurable 4/3/2 downstream ports
  - Upstream port supports both high-speed (HS) and full-speed (FS) traffic
  - Downstream ports support HS, FS, and low-speed (LS) traffic
  - 1 control pipe (endpoint 0, 64-byte data payload) and 1 interrupt pipe (endpoint 1, 1-byte data payload)
  - Backward compatible to USB specification revision 1.1
- Compliant with USB battery charging specification revision 1.2
  - Turning its downstream port from a standard downstream port (SDP) into charging downstream port (CDP) or Dedicated Charging Ports (DCP).
  - Enables portable device to charge from VBUS even when the USB bus is in suspend.
- On-chip 8-bit micro-processor
  - RISC-like architecture
  - USB optimized instruction set
  - Dual cycle instruction execution
  - Performance: 6 MIPS @ 12MHz
  - With 64-byte RAM and 4K internal ROM
  - Support customized PID, VID by reading external EEPROM
- Multiple Transaction translator (MTT)
  - MTT provides respective TT control logics for each downstream port.
- Each downstream port supports two-color status indicator, with automatic and manual modes compliant to USB specification revision 2.0
- Built-in upstream port 1.5KΩ pull-up and downstream port 15KΩ pull-down resistors
- Support both individual and gang modes of power management and over-current detection for downstream ports. Support both low/high-enabled power switches.
- Conform to bus power requirements of USB 2.0 specification
- Automatic switching between self-powered and bus-powered modes
- Integrate USB 2.0 transceiver
- Embedded PLL support external 12 MHz crystal / Oscillator clock input
- Optional 27/48 MHz Oscillator clock input (Only available in LQFP48 package)
- Support compound-device (non-removable in downstream ports) by I/O pin configuration (Only available in LQFP48 package)
- Number of Downstream port can be configured by GPIO without external EEPROM (Only available in LQFP48 package)
- Operate on 5V and 3.3V (Built-in 5V to 3.3V regulator)
- Internal power-fail detection for ESD recovery
- ESD protection up to 5KV of HBM (Human Body Model) by MIL-STD-883H standard
- Available package type: 48 pin LQFP, 28 pin QFN and 28 pin SSOP
- Applications:
  - Stand-alone USB hub / USB docking
  - UMPC/MID, motherboard on-board applications
  - Consumer electronics built-in hub application
  - Monitor built-in hub
  - Embedded systems
  - Compound device to support USB hub function such as keyboard hub applications

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

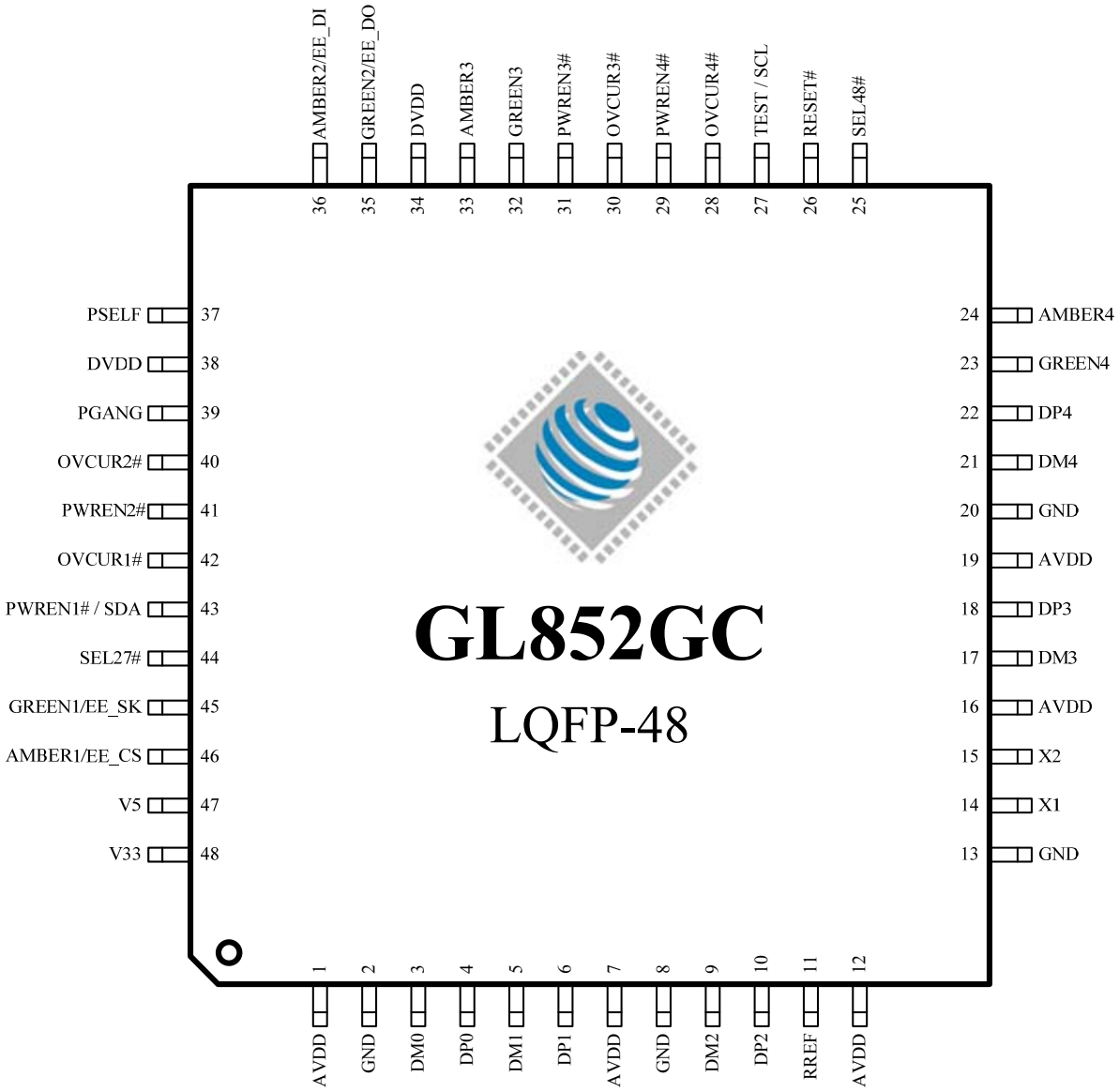


Figure 3.1 - GL852GC 48 Pin LQFP Pinout Diagram

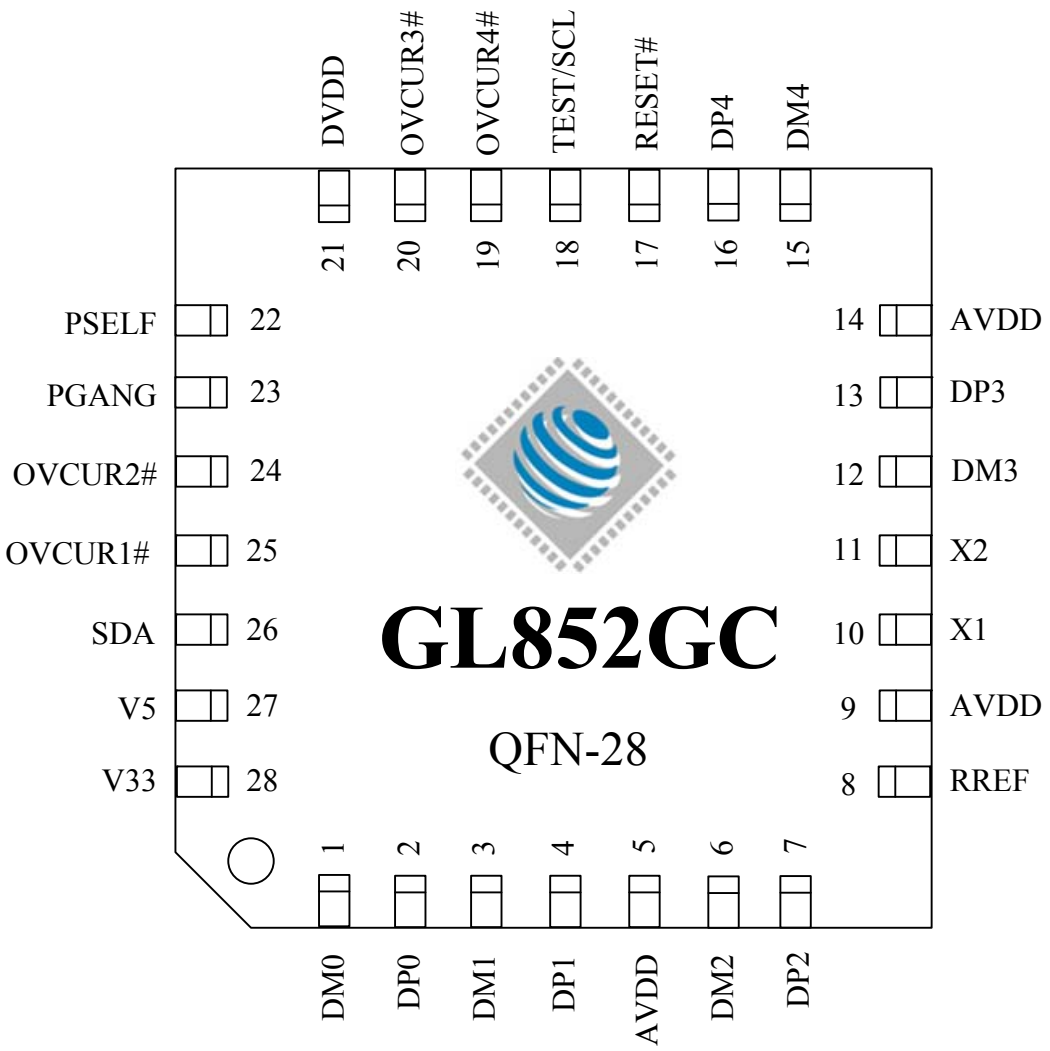


Figure 3.2 - GL852GC 28 Pin QFN Pinout Diagram

Figure 3.3 - GL852GC SSOP 28 Pin Pinout Diagram

3.2 Pin List

Table 3.1 - GL852GC LQFP 48 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	AVDD	P	13	GND	P	25	SEL48#	I	37	PSELF	I
2	GND	P	14	X1	I	26	RESET#	I	38	DVDD	P
3	DM0	B	15	X2	O	27	TEST / SCL	B	39	PGANG	B
4	DP0	B	16	AVDD	P	28	OVCUR4#	I	40	OVCUR2#	I
5	DM1	B	17	DM3	B	29	PWREN4#	O	41	PWREN2#	O
6	DP1	B	18	DP3	B	30	OVCUR3#	I	42	OVCUR1#	I
7	AVDD	P	19	AVDD	P	31	PWREN3#	O	43	PWREN1#/ SDA	B
8	GND	P	20	GND	P	32	GREEN3	O	44	SEL27#	I
9	DM2	B	21	DM4	B	33	AMBER3	O	45	GREEN1/EE_SK	O
10	DP2	B	22	DP4	B	34	DVDD	P	46	AMBER1/EE_CS	O
11	RREF	A	23	GREEN4	O	35	GREEN2/ EE_DO	O	47	V5	I/P
12	AVDD	P	24	AMBER4	O	36	AMBER2/ EE_DI	O	48	V33	O/P

Table 3.2 - GL852GC QFN 28 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DM0	B	8	RREF	A	15	DM4	B	22	PSELF	I_5V
2	DP0	B	9	AVDD	P	16	DP4	B	23	PGANG	B
3	DM1	B	10	X1	I	17	RESET#	I_5V	24	OVCUR2#	I_5V
4	DP1	B	11	X2	I	18	TEST/SCL	I/B	25	OVCUR1#	I_5V
5	AVDD	P	12	DM3	B	19	OVCUR4#	I_5V	26	SDA	O
6	DM2	B	13	DP3	B	20	OVCUR3#	I_5V	27	V5	I/P
7	DP2	B	14	AVDD	P	21	DVDD	P	28	V33	O/P

Table 3.3 - GL852GC SSOP 28 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	AVDD	P	8	DM3	B	15	GND	P	22	PWREN1#	O
2	DM2	B	9	DP3	B	16	DVDD	P	23	V5	I/P
3	DP2	B	10	AVDD	P	17	PSELF	I	24	V33	O/P
4	RREF	A	11	DM4	B	18	PGANG	B	25	DM0	B
5	AVDD	P	12	DP4	B	19	OVCUR2#	I	26	DP0	B
6	X1	I	13	RESET#	I	20	PWREN2#	O	27	DM1	B
7	X2	I	14	TEST/SCL	B/I	21	OVCUR1#	I	28	DP1	B

3.3 Pin Descriptions

Table 3.4 - Pin Descriptions

USB Interface					
Pin Name	GL852GC			I/O Type	Description
	LQFP 48 Pin	QFN 28 Pin	SSOP 28 Pin		
DM0,DP0	3,4	1,2	25,26	B	USB signals for USPORT
DM1,DP1	5,6	3,4	27,28	B	USB signals for DSPORT1
DM2,DP2	9,10	6,7	2,3	B	USB signals for DSPORT2
DM3,DP3	17,18	12,13	8,9	B	USB signals for DSPORT3
DM4,DP4	21,22	15,16	11,12	B	USB signals for DSPORT4
RREF	11	8	4	A	A 680Ω resister must be connected between RREF and analog ground (AGND).

Note: USB signals must be carefully handled in PCB routing. For detail information, please refer to **GL852GC Design Guideline**.

Hub Interface					
Pin Name	GL852GC			I/O Type	Description
	LQFP 48 Pin	QFN 28 Pin	SSOP 28 Pin		
OVCUR1#~4	42,40, 30,28	25,24, 20,19	21,19	I (pu)	Active low. Over current indicator for DSPORT1~4 OVCUR1# is the only over current flag for GANG mode.
PWREN1#~4	43,41, 31,29	-	22,20	O	Active low. Power enable output for DSPORT1~4 PWREN1# is the only power-enable output for GANG mode.
GREEN1~4	45,35, 32,23	-	-	1,3,4: O 2: B (pd)	Green LED indicator for DSPORT1~4 *GREEN[1~2] are also used to access the external EEPROM For detailed information, please refer to Chapter 5.
AMBER1~4	46,36, 33,24	-	-	O (pd)	Amber LED indicator for DSPORT1~4 *Amber [1~2] are also used to access the external EEPROM
PSELF	37	22	17	I	0: GL852GC is bus-powered. 1: GL852GC is self-powered.
PGANG	39	23	18	B	This pin is default put in input mode after power-on reset. Individual/gang mode is strapped during this period. After the strapping period, this pin will be set to output mode, and then output high for normal mode. When GL852GC is suspended, this pin will output low. *For detailed explanation, please see Chapter 5 Gang input:1, output: 0@normal, 1@suspend Individual input:0, output: 1@normal, 0@suspend

Clock and Reset Interface					
Pin Name	GL852GC			I/O Type	Description
	LQFP 48 Pin	QFN 28 Pin	SSOP 28 Pin		
X1	14	10	6	I	Crystal / OSC clock input
X2	15	11	7	O	Crystal clock output.
RESET#	26	17	13	I	Active low. External reset input, default pull high 10KΩ. When RESET# = low, whole chip is reset to the initial state.
SEL48#/SEL27#	25,44	--	-	I	SEL48#/SEL27#: 0 1: 48MHz OSC-in 1 0: 27MHz OSC-in 1 1: 12MHz X'tal/OSC-in

System Interface					
Pin Name	GL852GC			I/O Type	Description
	LQFP 48 Pin	QFN 28 Pin	SSOP 28 Pin		
TEST/SCL	27	18	14	I (pd) B	TEST: 0: Normal operation. 1: Chip will be put in test mode. I2C: clock output pin (QFN28/SSOP28 only)
SDA	--	26	-	B	I2C data pin

Power / Ground					
Pin Name	GL852GC			I/O Type	Description
	LQFP 48 Pin	QFN 28 Pin	SSOP 28 Pin		
AVDD	1,7,12, 16,19	5,9,14	1,5	P	3.3V analog power input for analog circuits.
DVDD	34,38	21	16	P	3.3V digital power input for digital circuits
GND	2,8, 13,20	-	15	P	Ground
V5	47	27	23	P / I	5V Power input. It need be NC if using external regulator
V33	48	28	24	P / O	5V-to-3.3V regulator Vout (LQFP48) 5V-to-3.3V regulator Vout & 3.3 input (QFN28) It can be NC or connect to 3.3V power if using external regulator (LQFP48 only)

Note: Analog circuits are quite sensitive to power and ground noise. PCB layout must take care the power routing and the ground plane. For detailed information, please refer to **GL852GC Design Guideline**.

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	P	Power / Ground
	P/I	5V Power, default input
	P/O	3.3V Power, default output
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

CHAPTER 4 BLOCK DIAGRAM

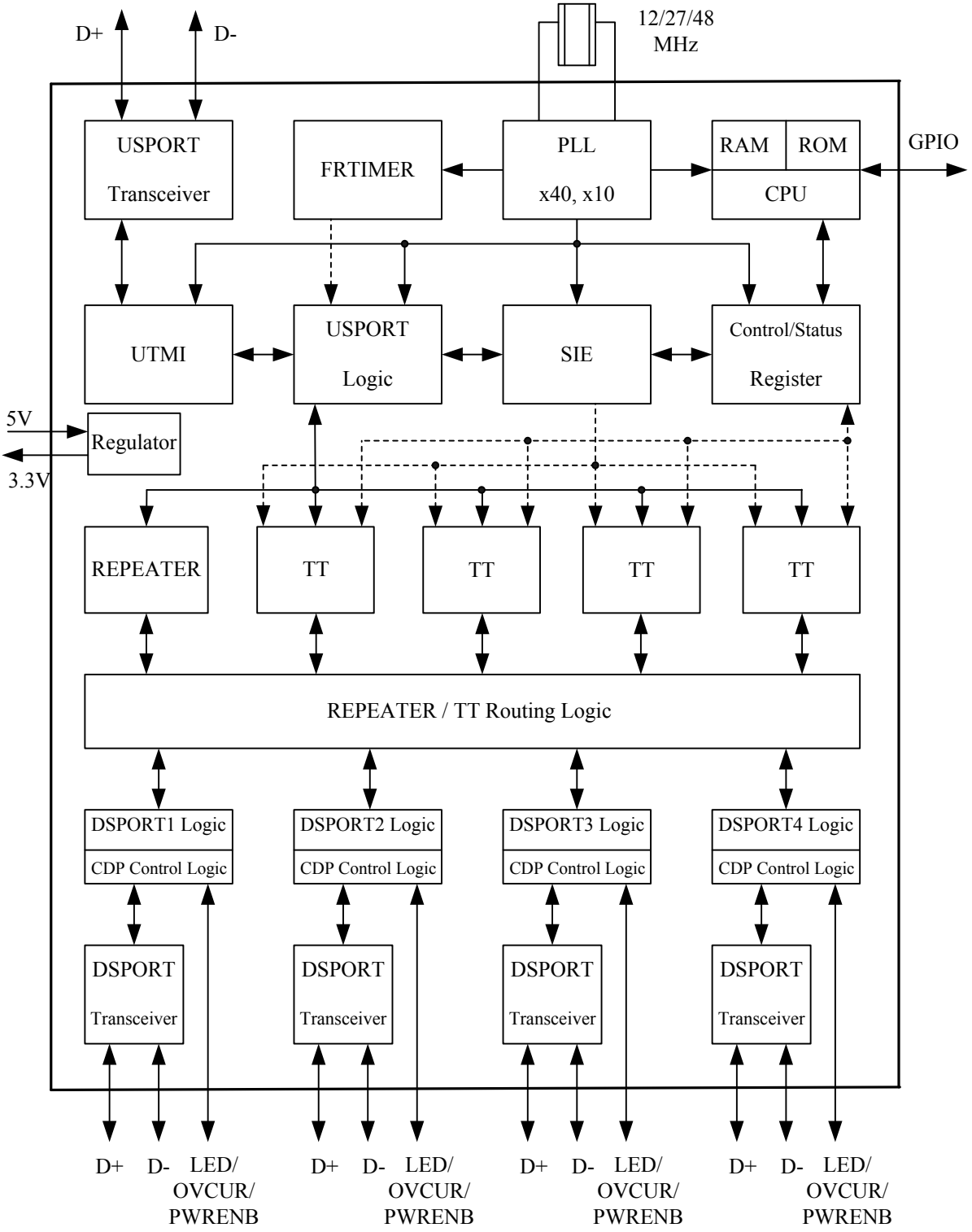


Figure 4.1 - GL852GC Block Diagram

CHAPTER 5 FUNCTION DESCRIPTION

5.1 General Description

5.1.1 USPORT Transceiver

USPORT (upstream port) transceiver is the analog circuit that supports both full-speed and high-speed electrical characteristics defined in chapter 7 of USB specification revision 2.0. USPORT transceiver will operate in full-speed electrical signaling when GL852GC is plugged into a 1.1 host/hub. USPORT transceiver will operate in high-speed electrical signaling when GL852GC is plugged into a 2.0 host/hub.

5.1.2 PLL (Phase Lock Loop)

GL852GC contains a 40x PLL. PLL generates the clock sources for the whole chip. The generated clocks are proven quite accurate that help in generating high speed signal without jitter.

5.1.3 FRTIMER

This module implements hub (micro)frame timer. The (micro)frame timer is derived from the hub's local clock and is synchronized to the host (micro)frame period by the host generated Start of (micro)frame (SOF). FRTIMER keeps tracking the host's SOF such that GL852GC is always safely synchronized to the host. The functionality of FRTIMER is described in section 11.2 of USB specification revision 2.0.

5.1.4 µC

µC is the micro-processor unit of GL852GC. It is an 8-bit RISC processor with 2K ROM and 64 bytes RAM. It operates at 6MIPS of 12 MHz clock to decode the USB command issued from host and then prepares the data to respond to the host. In addition, µC can handle GPIO (general purpose I/O) settings and reading content of EEPROM to support high flexibility for customers of different configurations of hub. These configurations include self/bus power mode setting, individual/gang mode setting, downstream port number setting, device removable/non-removable setting, and PID/VID setting.

5.1.5 UTMI (USB 2.0 Transceiver Microcell Interface)

UTMI handles the low level USB protocol and signaling. It's designed based on the Intel's UTMI specification 1.01. The major functions of UTMI logic are to handle the data and clock recovery, NRZI encoding/decoding, Bit stuffing /de-stuffing, supporting USB 2.0 test modes, and serial/parallel conversion.

5.1.6 USPORT Logic

USPORT implements the upstream port logic defined in section 11.6 of USB specification revision 2.0. It mainly manipulates traffics in the upstream direction. The main functions include the state machines of Receiver and Transmitter, interfaces between UTMI and SIE, and traffic control to/from the REPEATER and TT.

5.1.7 SIE (Serial Interface Engine)

SIE handles the USB protocol defined in chapter 8 of USB specification revision 2.0. It co-works with μC to play the role of the hub kernel. The main functions of SIE include the state machine of USB protocol flow, CRC check, PID error check, and timeout check. Unlike USB 1.1, bit stuffing/de-stuffing is implemented in UTMI, not in SIE.

5.1.8 Control/Status Register

Control/Status register is the interface register between hardware and firmware. This register contains the information necessary to control endpoint0 and endpoint1 pipelines. Through the firmware based architecture, GL852GC possesses higher flexibility to control the USB protocol easily and correctly.

5.1.9 REPEATER

Repeater logic implements the control logic defined in section 11.4 and section 11.7 of USB specification revision 2.0. REPEATER controls the traffic flow when upstream port and downstream port are signaling in the same speed. In addition, REPEATER will generate internal resume signal whenever a wakeup event is issued under the situation that hub is globally suspended.

5.1.10 TT

TT(Transaction Translator) implements the control logic defined in section 11.14 ~ 11.22 of USB specification revision 2.0. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub. GL852GC adopts multiple TT architecture to provide the most performance effective solution. Multiple TT provides control logics for each downstream port respectively.

5.1.11 REPEATER/TT Routing Logic

REPEATER and TT are the major traffic control machines in the USB 2.0 hub. Under situation that USPORT and DSPORT are signaling in the same speed, REPEATER/TT routing logic switches the traffic channel to the REPEATER. Under situation that USPORT is in the high speed signaling and DSPORT is in the full/low speed signaling, REPEATER/TT routing logic switches the traffic channel to the TT.

5.1.11.1 Connected to 1.1 Host/Hub

If an USB 2.0 hub is connected to the downstream port of an USB 1.1 host/hub, it will operate in USB 1.1 mode. For an USB 1.1 hub, both upstream direction traffic and downstream direction traffic are passing through REPEATER. That is, the REPEATER/TT routing logic will route the traffic channel to the REPEATER.

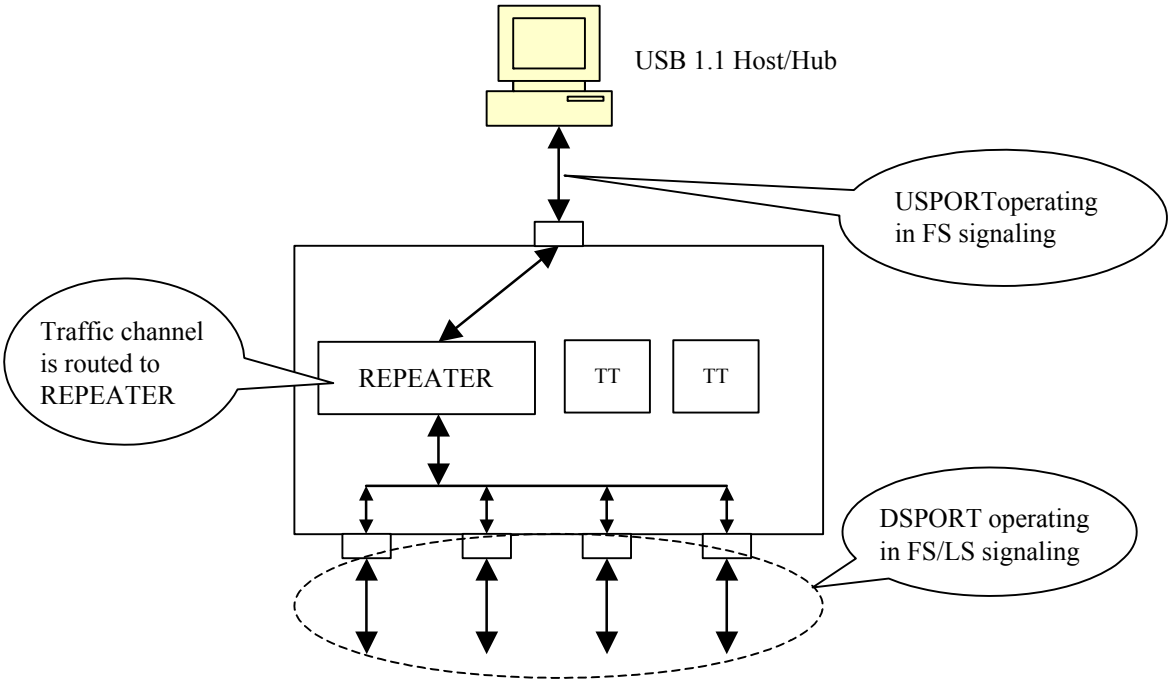


Figure 5.1 - Operating in USB 1.1 Schemes

5.1.11.2 Connected to USB 2.0 Host/Hub

If an USB 2.0 hub is connected to an USB 2.0 host/hub, it will operate in USB 2.0 mode. The upstream port signaling is in high speed with bandwidth of 480 Mbps under this environment. The traffic channel will then be routed to the REPEATER when the device connected to the downstream port is signaling also in high speed. On the other hand, the traffic channel will then be routed to TT when the device connected to the downstream port is signaling in full/low speed.

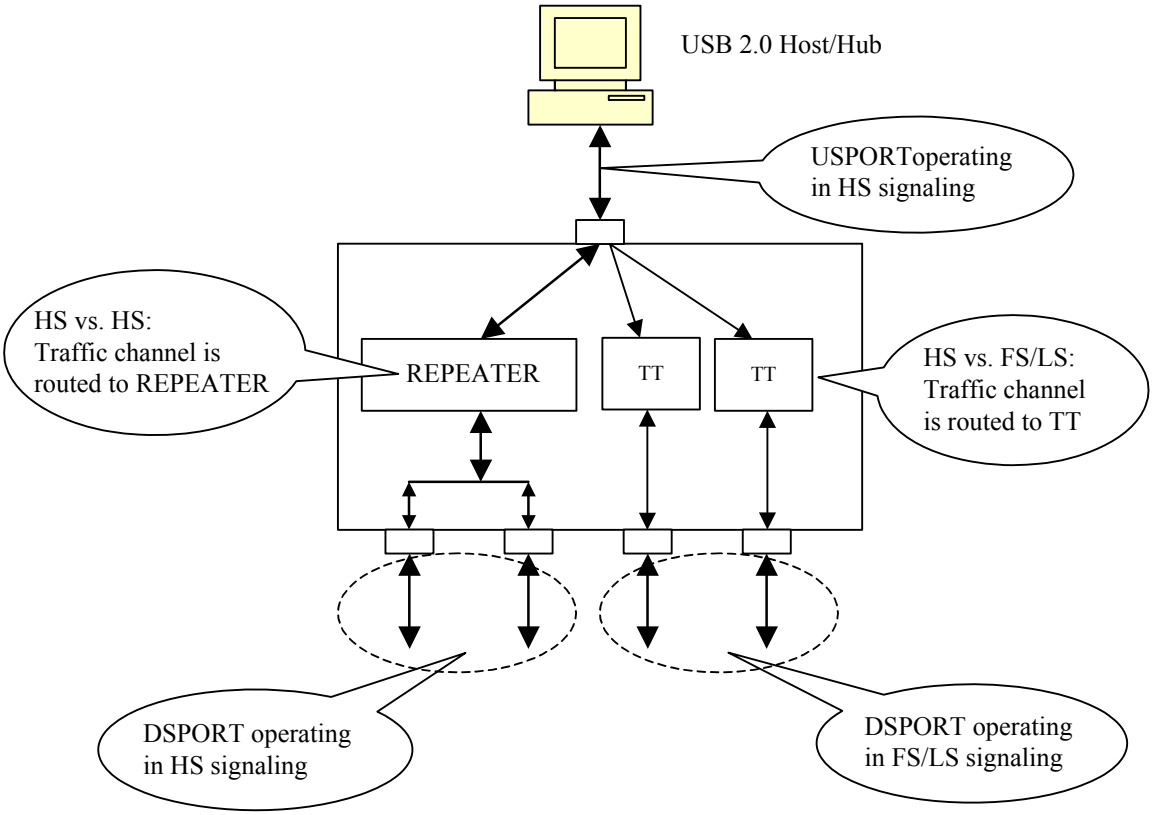


Figure 5.2 - Operating in USB 2.0 Schemes

5.1.12 DSPORT Logic

DSPORT (downstream port) logic implements the control logic defined in section 11.5 of USB specification revision 2.0. It mainly manipulates the state machine, the connection/disconnection detection, over current detection and power enable control, and the status LED control of the downstream port. Besides, it also output the control signals to the DSPORT transceiver.

5.1.13 CDP Control Logic

CDP (charging downstream port) control logic implements the logic defined in USB Battery charging specification revision 1.2. The major function of it is to control DSPORT Transceiver to make handshake with a portable device which is compliant with USB Battery charging spec rev1.2 as well. After recognizing charging detection each other, portable device will draw 900mA or 1.5A from VBUS to fast charge its battery.

5.1.14 DSPORT Transceiver

DSPORT transceiver is the analog circuit that supports high-speed, full-speed, and low-speed electrical characteristics defined in chapter 7 of USB specification revision 2.0. In addition, each DSPORT transceiver accurately controls its own squelch level to detect the detachment and attachment of devices.

5.1.15 Regulator

GL852GC build in internal regulator converts 5V input to 3.3V output.

5.2 Configuration and I/O Settings

5.2.1 RESET Setting

GL852GC's power on reset can either be triggered by external reset or internal power good reset circuit. The external reset pin, RESETJ, is connected to upstream port Vbus (5V) to sense the USB plug / unplug or 5V voltage drop. The reset trigger voltage can be set by adjusting the value of resistor R1 and R2 (Suggested value refers to schematics) GL852GC's internal reset is designed to monitor silicon's internal core power (3.3V) and initiate reset when unstable power event occurs. The power on sequence will start after the power good voltage has been met, and the reset will be released after approximately 2.7 μS after power good. GL852GC's reset circuit as depicted in the picture

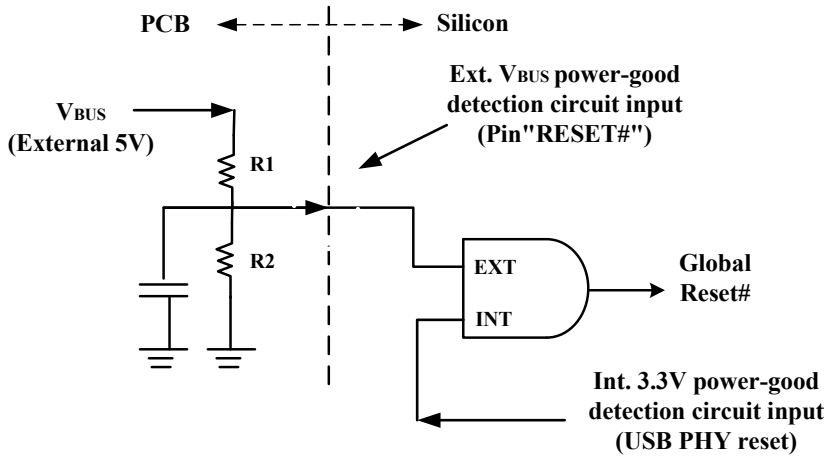


Figure 5.3 - Power on Reset Diagram

To fully control the reset process of GL852GC, we suggest the reset time applied in the external reset circuit should longer than that of the internal reset circuit. Timing of POR is illustrated as below figure.

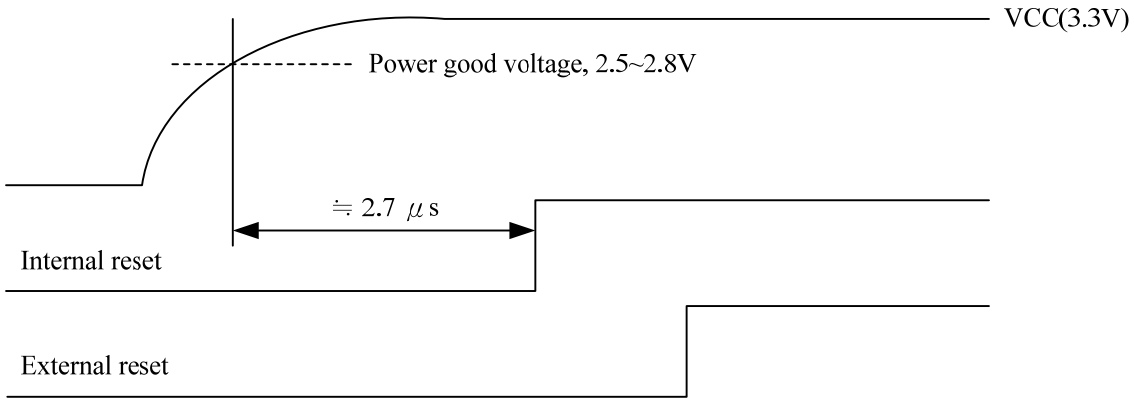


Figure 5.4 - Power on Sequence of GL852GC

5.2.2 PGANG Setting

To save pin count, GL852GC uses the same pin to decide individual/gang mode as well as to output the suspend flag. The individual/gang mode is decided within 20us after power on reset. Then, about 50ms later, this pin is changed to output mode. GL852GC outputs the suspend flag once it is globally suspended. For individual mode, a pull low resister greater than 100KΩ should be placed. For gang mode, a pull high resister which greater than 100KΩ should be placed. In figure 5.6, we also depict the suspend LED indicator schematics. It should be noticed that the polarity of LED must be followed, otherwise the suspend current will be over spec limitation (2.5mA).

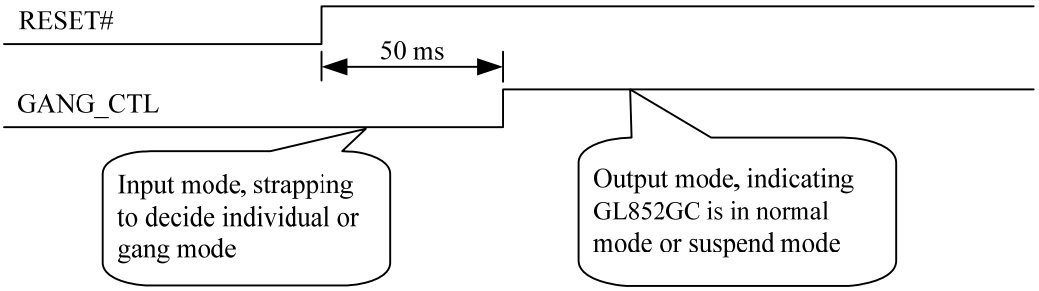


Figure 5.5 - Timing of PGANG Strapping

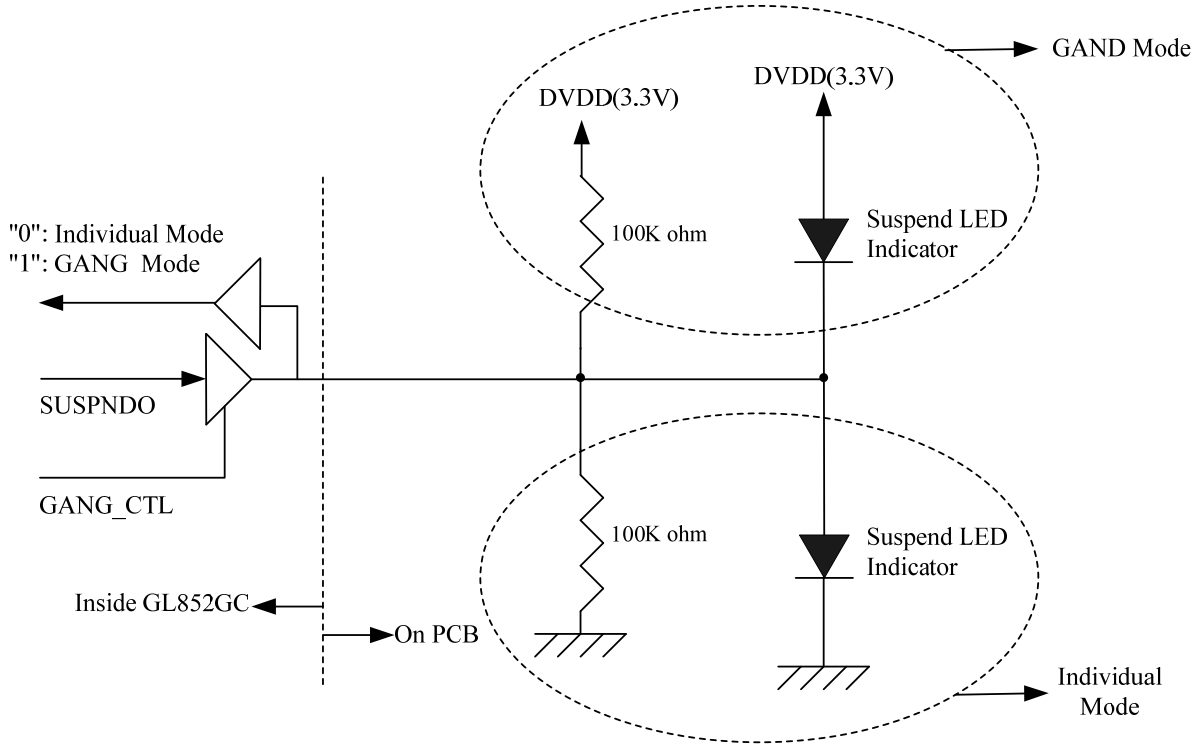


Figure 5.6 - GANG Mode Setting

5.2.3 SELF/BUS Power Setting

By setting PSELF, GL852GC can be configured as a bus-power or a self-power hub.

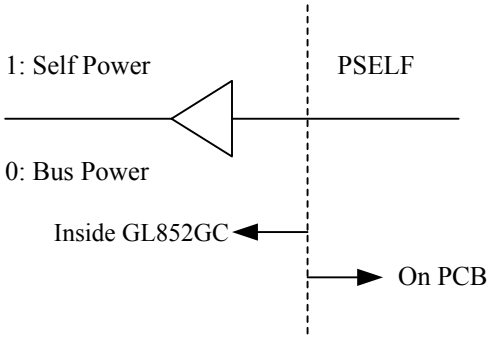


Figure 5.7 - SELF/BUS Power Setting

5.2.4 LED Connections

GL852GC controls the LED lighting according to the flow defined in section 11.5.3 of Universal Serial Bus Specification Revision2.0. Both manual mode and Automatic mode are supported in GL852GC. When GL852GC is globally suspended, GL852GC will turn off the LED to save power.

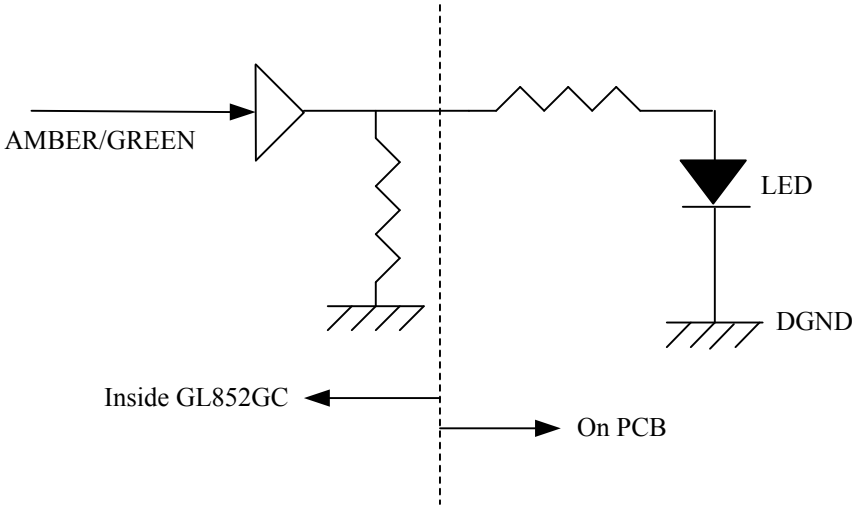


Figure 5.8 - LED Connection

5.2.5 EEPROM Setting

GL852GC replies to host commands by the default settings in the internal ROM. GL852GC also offers the ability to reply to the host according to the settings in the external EEPROM (LQFP48 supports both 93C46 and 24C02; QFN28/SSOP28 only supports 24C02). And to prevent the content of EEPROM from being over-written, amber LED will be disabled when EEPROM exists. The detail setting information please refers to the **GL852GC AP Note_EEPROM Info** document.

5.2.6 Power Switch Enable Polarity (Only Available for LQFP 48 Package)

Both low/high-enabled power switches are supported. It is determined by jumper setting, based on the state of pin AMBER2, as the following table:

Table 5.1 - Configuration by Power Switch Type

AMBER2	Power Switch Enable Polarity
0	Low-active
1	High-active

Note: When AMBER2=1, the external resistor of PWREN1~4 need pull down

5.2.7 Port Number Configuration (Only Available for LQFP 48 Package)

Number of downstream port can be configured as 1/2/3/4 ports by pin strapping in addition to EEPROM, based on the state of pin AMBER 3, AMBER 4, as the following table:

Table 5.2 - Port Number Configuration

AMBER3	AMBER 4	# of DP Declaration
1	1	1 (Port1)
1	0	2 (Port1/2)
0	1	3 (Port1/2/3)
0	0	4 (Port1/2/3/4)

5.2.8 Non-removable Port Configuration (Only Available for LQFP 48 Package)

For compound application or embedded system, downstream ports that always connected inside the system can be set as non-removable based on the state of corresponding status LED, pin GREEN 1~4. If the pin is pull high in the initial stage (POR reset), the corresponding port will be set as non-removable.

5.2.9 Reference Clock Configuration (Only Available for LQFP 48 Package)

GL852GC can support optional 27/48MHz clock source, which is selectable through GPIO configurations. For some on-board design that 27/48MHz clock source is available, such as motherboard or Monitor built-in applications, system integrator can leverage this feature to further reduce BOM cost by removing external crystal.

Table 5.3 - Ref. Clock Configuration

SEL48	SEL27	Clock Source
0	1	48MHz OSC-in
1	0	27MHz OSC-in
1	1	12MHz X’tal/OSC-in

CHAPTER 6 USB-IF BATTERY CHARGING SPECIFICATION REV.1.2 SUPPORT

6.1 Background

The USB ports on personal computers are convenient places for portable devices to draw current for charging their batteries. This convenience has led to the creation of dedicated chargers that simply expose a USB standard-A receptacle. This allows portable devices to use the same USB cable to charge from either a PC or from a dedicated charger.
If a portable device is attached to a USB host or hub, then the USB 2.0 specification requires that after connecting, a portable device must draw less than:

- 2.5 mA average if the bus is suspended
- 100 mA maximum if bus is not suspended and not configured
- 500 mA maximum if bus is not suspended and configured for 500 mA

If a portable device is attached to a charging host or hub, it is allowed to draw a current up to 1.5A, regardless of suspend. In order for a portable device determine how much current it is allowed to draw from an upstream USB port, the USB-IF Battery Charging specification defines the mechanisms that allow the portable device to distinguish between either a USB standard host, hub or a USB charging host. Since portable device can be attached to USB charging ports from various manufactures, it is important that all USB charging ports behave the same way. This specification also defines the requirements for a USB chargers and charging downstream ports.

6.2 Charging Downstream Port (CDP)

GL852GC supports battery charging detection, turning its downstream port from a standard downstream port (SDP) into charging downstream port (CDP). GL852GC will make physical layer handshaking when a portable device (PD) compliant with BC rev1.2 attaches to its downstream port. After physical layer handshaking, PD is allowed to draw more current up to 900mA or 1.5A, depending on PD is configured as High-Speed (900mA) or Full-Speed/Low-Speed (1.5A) device.

6.3 Charging Detection Hardware Handshaking

Once the charging downstream port of GL852GC enabled, it will monitor the V_{DP_SRC} on D+ line anytime. When BCv1.2 compliant PD attached to the downstream port, it will drive V_{DP_SRC} on D+ line to initiate handshaking with charging downstream port. GL852GC will response on its D- line by V_{DM_SRC} and keep in a certain period of time and voltage level. The portable device will accept this handshake on its D- line in correct timing period and voltage level and then turns off its V_{DP_SRC} on D+ line. GL852GC will recognize that charging negotiation is finished by counting time between PD turning on and off its V_{DP_SRC}. After that, the portable device can start to draw more current at VBUS to charge its battery more rapidly. It can draw current up to 1.5A or 900mA, depending on PD is configured as HS, FS or LS device.

If no response on D- line returns, the portable device will recognize that it is attached to a standard downstream port, not a charging port.

6.4 Dedicated Charging Port (DCP)

GL852GC also support dedicated charging port, which is a downstream port on a device that outputs power through a USB connector, but is not capable of enumerating a downstream device. With the adequate system circuit design, GL852GC will turn its downstream port from a standard downstream port (SDP) into dedicated charging port (DCP), i.e short the D+ line to the D- line, to let PD draw current up to 1.5A. The detail system design information please refers to the **GL852GC Design Guide** document.

6.5 Port Numbers of Charging Downstream Port Configuration

Numbers of charging downstream port can be configured as 1/2/3/4 ports by pin strapping based on the state of pin AMBER1, GREEN4, as the following table **(for LQFP48 Package only)**:

Table 6.4 - CDP Port Number Configuration

AMBER1	GREEN4	CDP port #
NC	NC	Port1
NC	1	Port1/2
1	NC	Port 1/2/3
1	1	Port 1/2/3/4

For QFN28 package, Port1is default set as charging downstream port. For other configuration, need to use EEPROM. EEPROM setting (93C46/24C02) for both LQFP48 and QFN28 is as follows:
Hub Charging (0Ah): need set Bit6=1 before enable charging function of each downstream port

Bit 0: Port1 battery charging function enable

0	Standard Downstream Port (Default)
1	Charging Downstream Port

Bit 1: Port2 battery charging function enable

0	Standard Downstream Port (Default)
1	Charging Downstream Port

Bit 2: Port3 battery charging function enable

0	Standard Downstream Port (Default)
1	Charging Downstream Port

Bit 3: Port4 battery charging function enable

0	Standard Downstream Port (Default)
1	Charging Downstream Port

Note: Bit0 - 3 are valid only when Bit6 = 1

Bit 6: Hub battery charging function enable

0	Disable charging downstream port (Default)
1	Enable charging downstream port

The detail setting information please refers to the **GL852GC AP Note_EEPROM Info** document.

CHAPTER 7 ELECTRICAL CHARACTERISTICS

7.1 Maximum Ratings

Table 7.1 - Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_5	5V Power Supply	-0.5	+6.0	V
V_{DD}	3.3V Power Supply	-0.5	+3.6	V
V_{IN}	3.3V Input Voltage for digital I/O(EE_DO) pins	-0.5	+3.6	V
V_{INOD}	Open-Drain Input (Ovcur1-4,Pself,Reset)	-0.5	+5.5	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	-0.5	+3.6	V
T_S	Storage Temperature under bias	-60	+100	°C
F_{OSC}	Frequency	12 MHz ± 0.05%		

7.2 Operating Ranges

Table 7.2 - Operating Ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_5	5V Power Supply	4.5	5.0	5.5	V
V_{DD}	3.3V Power Supply	3.0	3.3	3.6	V
V_{IND}	Input Voltage for digital I/O pins	-0.5	3.3	3.6	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	0.5	3.3	3.6	V
T_A	Ambient Temperature	0	-	70	°C
T_J	Absolute maximum junction temperature	0	-	125	°C
θ JA	Thermal Characteristics LQFP 48	-	78.7	-	oC/W
	Thermal Characteristics QFN 28	-	33.3	-	oC/W
	Thermal Characteristics SSOP 28		61.6		oC/W

7.3 DC Characteristics

Table 7.3 - DC Characteristics except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
P_D	Power Dissipation	-	-	449.5	mW
V_{DD}	Power Supply Voltage	3	3.3	3.6	V
V_{IL}	LOW level input voltage	-	-	0.8	V
V_{IH}	HIGH level input voltage	2.0	-	-	V
V_{TLH}	LOW to HIGH threshold voltage	1.4	1.5	1.6	V
V_{THL}	HIGH to LOW threshold voltage	0.87	0.94	0.99	V
V_{OL}	LOW level output voltage when I_{OL}=8mA	-	-	0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4	-	-	V
I_{OLK}	Leakage current for pads with internal pull up or pull down resistor	-	-	30	μA
R_{DN}	Pad internal pull down resister	29K	59K	135K	Ω
R_{UP}	Pad internal pull up resister	80K	108K	140K	Ω

Table 7.4 - DC Characteristics of USB Signals under FS/LS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	DP/DM static output LOW	0	-	0.3	V
V_{OH}	DP/DM static output HIGH	2.8	-	3.6	V
V_{DI}	Differential input sensitivity	0.2	-	-	V
V_{CM}	Differential common mode range	0.8	-	2.5	V
V_{SE}	Single-ended receiver threshold	0.2	-	-	V
C_{IN}	Transceiver capacitance	-	-	20	pF
I_{LO}	Hi-Z state data line leakage	-10	-	+10	μA
Z_{DRV}	Driver output resistance	28	-	44	Ω

Table 7.5 - DC Characteristics of USB Signals under HS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	DP/DM static output LOW	-	-	0.1	V
C_{IN}	Transceiver capacitance	4	4.5	5	pF
I_{LO}	Hi-Z state data line leakage	-5	0	+5	μA
Z_{DRV}	Driver output resistance for USB 2.0 HS	48	45	42	Ω

7.4 Power Consumption

Table 7.6 - DC Supply Current

Symbol	Condition			Internal Regulator	Unit
	Active ports	Host	Device		
I_{SUSP}	Suspend			784	uA
I_{CC}	4	F*1	F	89.9	mA
		H*1	H	81.6	mA
		H	F	87.6	mA
	3	F	F	78.9	mA
		H	H	72.6	mA
		H	F	76.3	mA
	2	F	F	67.7	mA
		H	H	61.6	mA
		H	F	65.3	mA
	1	F	F	56.9	mA
		H	H	52	mA
		H	F	54.4	mA
	No Active	F	N/A	42.5	mA
		H	N/A	43.9	mA

*: F: Full-Speed, H: High-Speed

Note:

Test result represents silicon level operating current, without considering additional power consumption contributed by external over-current protection circuit such as power switch or polyfuse.

7.5 AC Characteristics

GL852GC LQFP 48 pin package can support both 93C46 & 24C02 type EEPROM for customized VID/PID. GL852GC QFN28/SSOP28 pin package can only support 24C02 type EEPROM. AC characteristics of these two types of EEPROM summarized as below figures and tables.

7.5.1 93C46 EEPROM IF

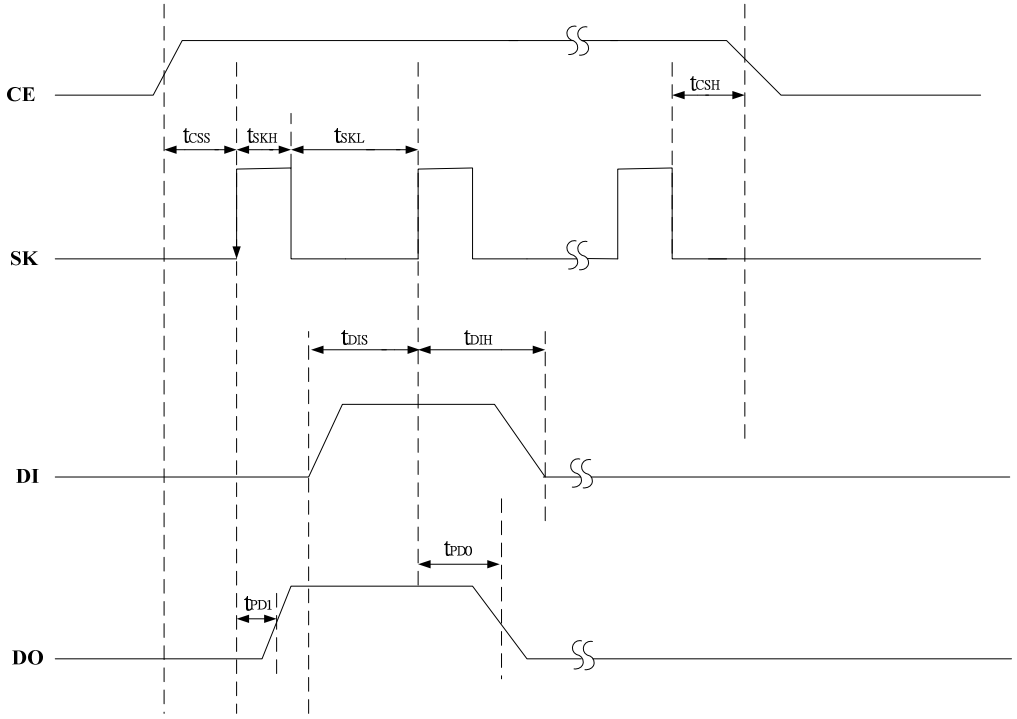
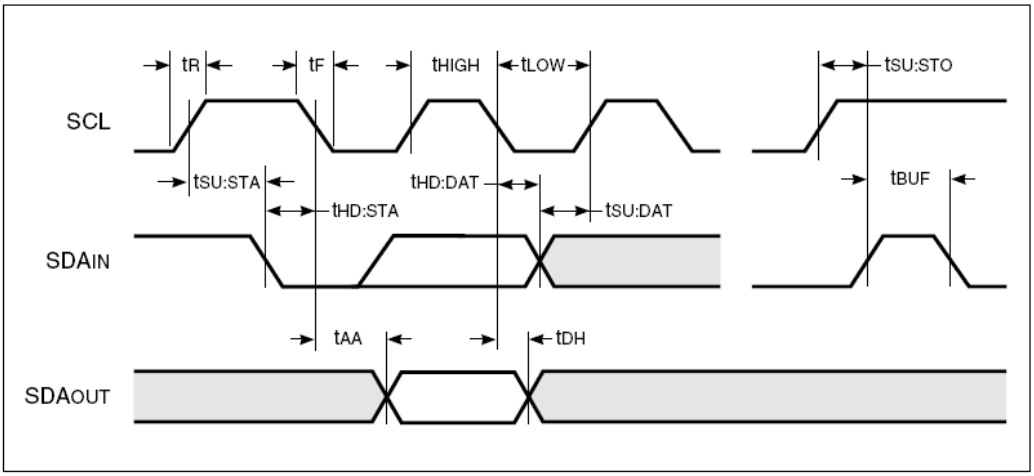


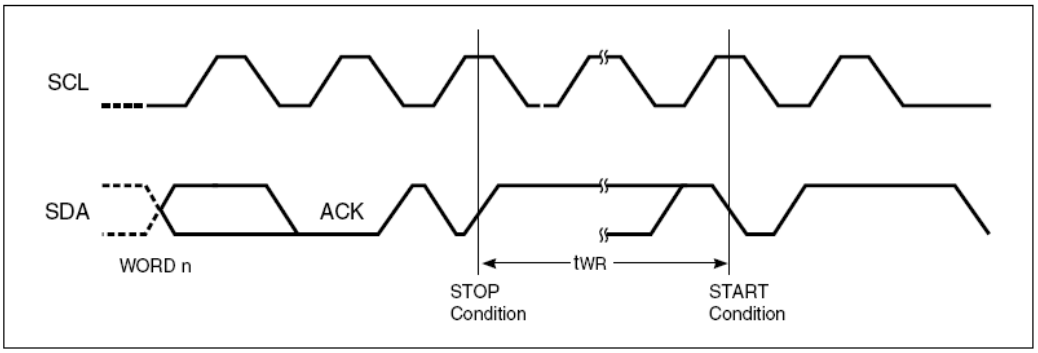
Table 7.7 - AC Characteristics of EEPROM Interface (93C46)

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CSS}	CS Setup Time	3.0			us
t_{CSH}	CS Hold Time	3.0			
t_{SKH}	SK High Time	1.0			
t_{SKL}	SK Low Time	2.2			
t_{DIS}	DI Setup Time	1.8			
t_{DIH}	DI Hold Time	2.4			
t_{PD1}	Output Delay to “1”			1.8	
t_{PD0}	Output Delay to “0”			1.8	

7.5.2 24C02 EEPROM Interface



Bus Timing



Write Cycle Timing

Table 7.8 - AC Characteristics of EEPROM Interface (24C02)

Symbol	Parameter	Test Conditions	1.8V-5.5V Min.	1.8V-5.5V Max.	2.5V-5.5V Min.	2.5V-5.5V Max.	Unit
f_{SCL}	SCL Clock Frequency		0	100	0	400	KHz
T	Noise Suppression Time(1)		—	100	—	50	ns
t_{LOW}	Clock LOW Period		4.7	—	1.2	—	µs
t_{HIGH}	Clock HIGH Period		4	—	0.6	—	µs
t_{BUF}	Bus Free Time Before New Transmission(1)		4.7	—	1.2	—	µs
$t_{SU:STA}$	Start Condition Setup Time		4.7	—	0.6	—	µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7	—	0.6	—	µs
$t_{HD:STA}$	Start Condition Hold Time		4	—	0.6	—	µs
$t_{HD:STO}$	Stop Condition Hold Time		4	—	0.6	—	µs
$t_{SU:DAT}$	Data In Setup Time		200	—	100	—	ns
$t_{HD:DAT}$	Data In Hold Time		0	—	0	—	ns
t_{DH}	Data Out Hold Time	SCL LOW to SDA Data Out Change	100	—	50	—	ns
t_{AA}	Clock to Output	SCL LOW to SDA Data Out Valid	0.1	4.5	0.1	0.9	µs
t_R	SCL and SDA Rise Time(1)		—	1000	—	300	ns
t_F	SCL and SDA Fall Time(1)		—	300	—	300	ns
t_{WR}	Write Cycle Time		—	10	—	5	ms

Note:
1. This parameter is characterized but not 100% tested.

7.6 On-Chip Power Regulator

GL852GC requires 3.3V source power for normal operation of internal core logic and USB physical layer (PHY). The integrated low-drop power regulator converts 5V power input from USB cable (Vbus) to 3.3V voltage for silicon power source. The 3.3V power output is guaranteed by an internal voltage reference circuit to prevent unstable 5V power compromise USB data integrity. The regulator's maximum current loading is 200mA, which provides enough tolerance for normal GL852GC operation (below 100mA).

On-chip Power Regulator Features:

- 5V to 3.3V low-drop power regulator
- 200mA maximum output driving capability
- Provide stable 3.3V output when Vin = 3.4V~5.5V
- Max. suspend current:190uA; typical suspend current 164uA.

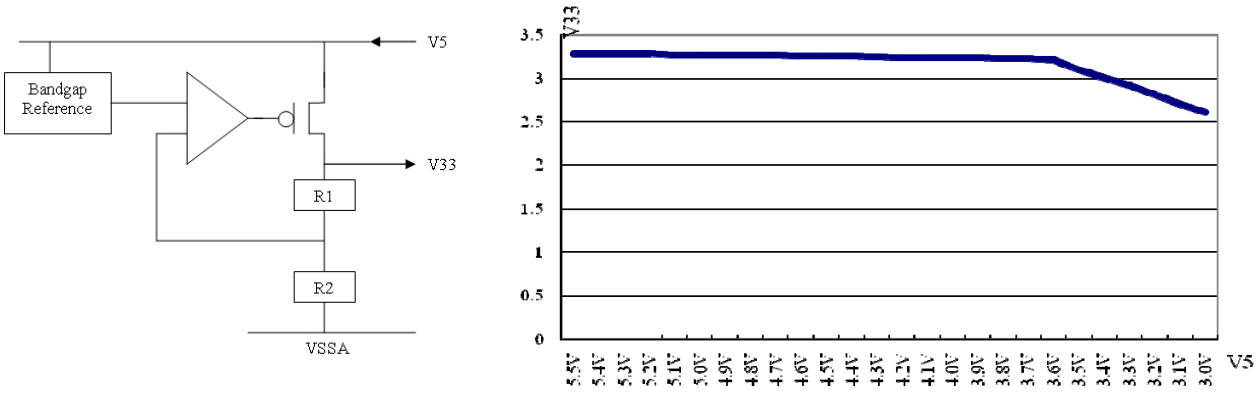


Figure 7.1 - Vin(V5) vs Vout(V33)*

*Note: Measured environment: Ambient temperature = 25℃ / Current Loading = 200mA

CHAPTER 8 PACKAGE DIMENSION

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	1.60 (63.0)
A1	0.05 (2.0)	---	0.15 (5.9)
A2	1.35 (53.1)	1.40 (55.1)	1.45 (57.1)
b	0.17 (6.7)	0.22 (8.7)	0.27 (10.6)
b1	0.17 (6.7)	0.20 (7.9)	0.23 (9.1)
c	0.09 (3.5)	---	0.20 (7.9)
c1	0.09 (3.5)	---	0.16 (6.3)
D	9.00 (354.3) BSC		
D1	7.00 (275.6) BSC		
e	0.50 (19.7) BSC		
E	9.00 (354.3) BSC		
E1	7.00 (275.6) BSC		
L	0.45 (17.7)	0.60 (23.6)	0.75 (29.5)
L1	1.00 (39.4) REF		
R1	0.08 (3.1)	---	---
R2	0.08 (3.1)	---	0.20 (7.9)
S	0.20 (7.9)	---	---
aaa	0.20 (7.9)		
bbb	0.20 (7.9)		
ccc	0.08 (3.1)		
ddd	0.08 (3.1)		
θ	0°	3.5°	7°
θ1	0°	---	---
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTE: 1. REFER TO JEDEC MS-026/BBC
2. ALL DIMENSIONS IN MILLIMETERS.

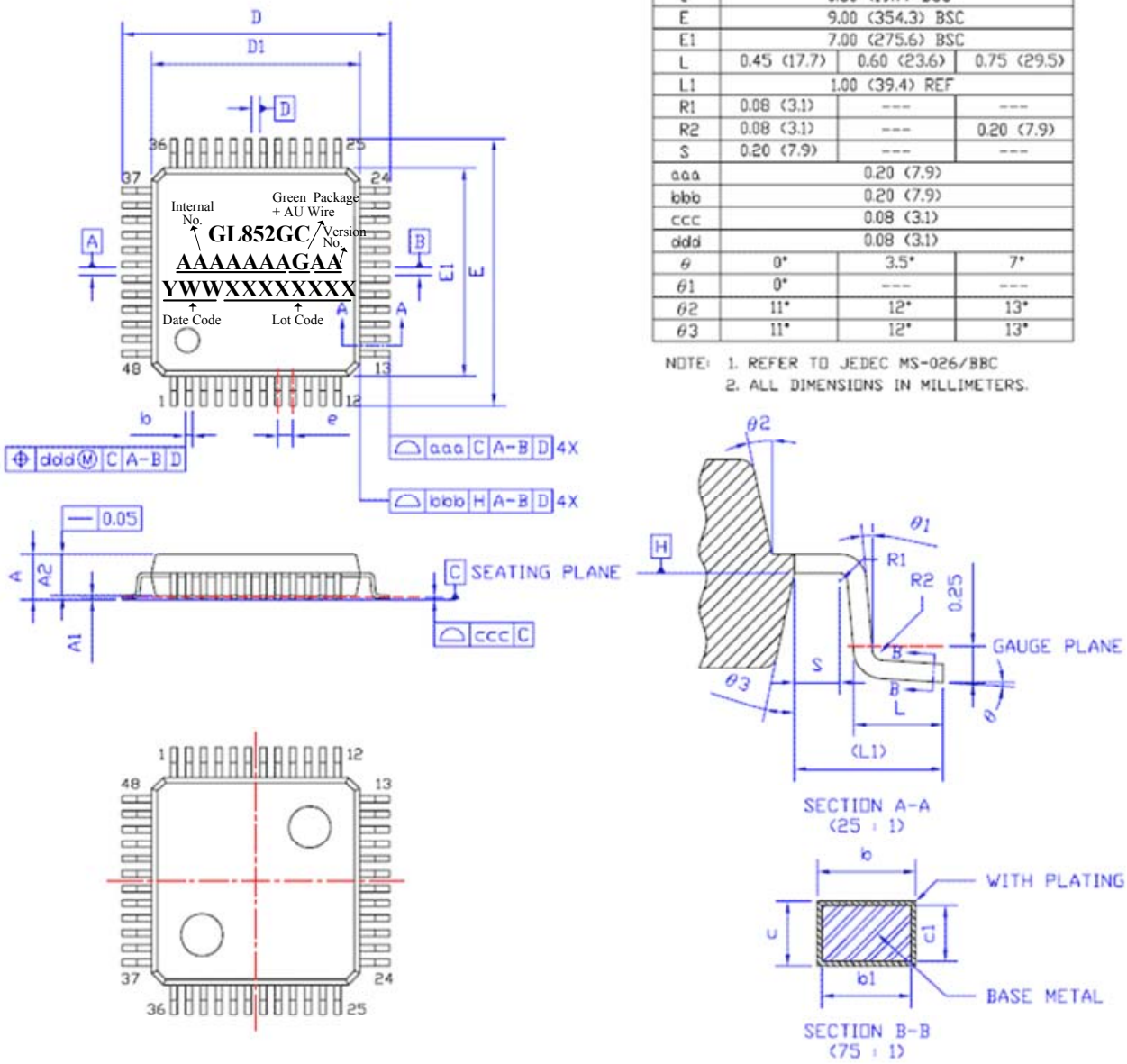
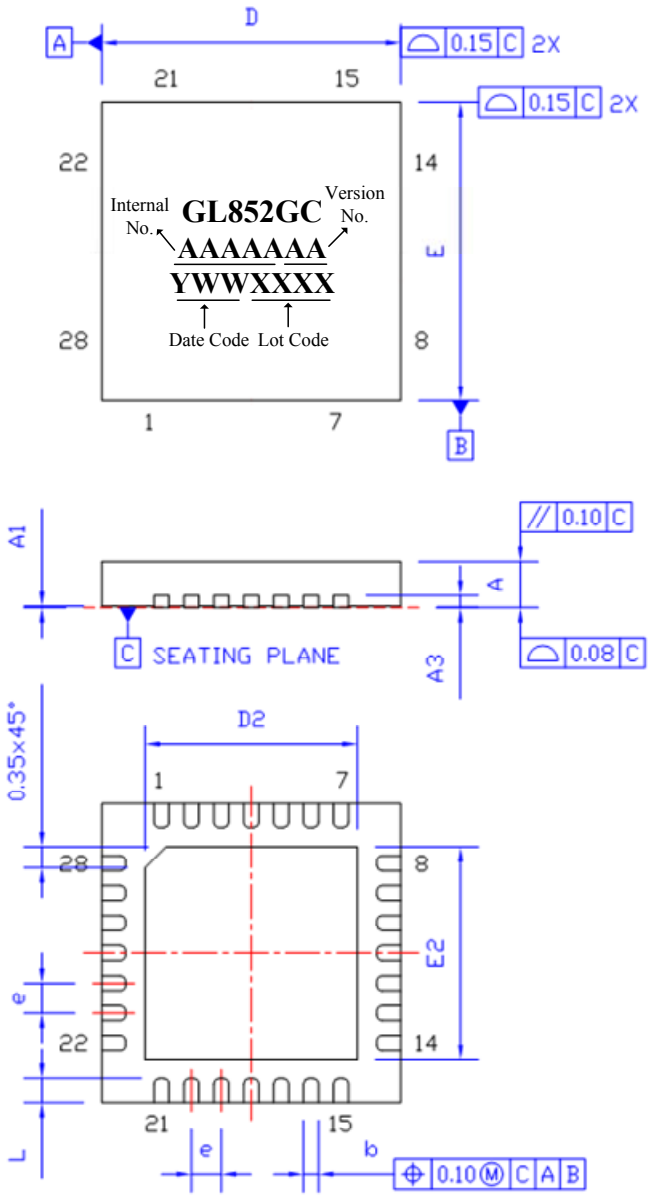


Figure 8.1 - GL852GC 48 Pin LQFP Package



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.18 (7.1)	0.25 (9.8)	0.30 (11.8)
D	5.00 (196.9) BSC		
D2	3.40 (133.9)	3.55 (139.8)	3.70 (145.7)
E	5.00 (196.9) BSC		
E2	3.40 (133.9)	3.55 (139.8)	3.70 (145.7)
e	0.50 (19.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

Figure 8.2 - GL852GC 28 Pin QFN Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	2.00 (78.7)
A1	0.05 (2.0)	---	0.21 (8.3)
A2	1.65 (65.0)	1.75 (68.9)	1.85 (72.8)
b	0.22 (8.7)	---	0.38 (15.0)
b1	0.22 (8.7)	0.30 (11.8)	0.33 (13.0)
c	0.09 (3.5)	---	0.25 (9.8)
c1	0.09 (3.5)	---	0.21 (8.3)
D	10.20 (401.6) BSC		
e	0.65 (25.6) BSC		
E	7.80 (307.1) BSC		
E1	5.30 (208.7) BSC		
L	0.55 (21.7)	0.75 (29.5)	0.95 (37.4)
L1	1.25 (49.2) REF		
R1	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
R2	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
y	---	---	0.08 (3.1)
θ	0°	4°	8°
θ1	0°	---	---
θ2	7° TYP		
θ3	7° TYP		

NOTE: 1. REFER TO JEDEC MO-150
2. ALL DIMENSIONS IN MILLIMETERS.

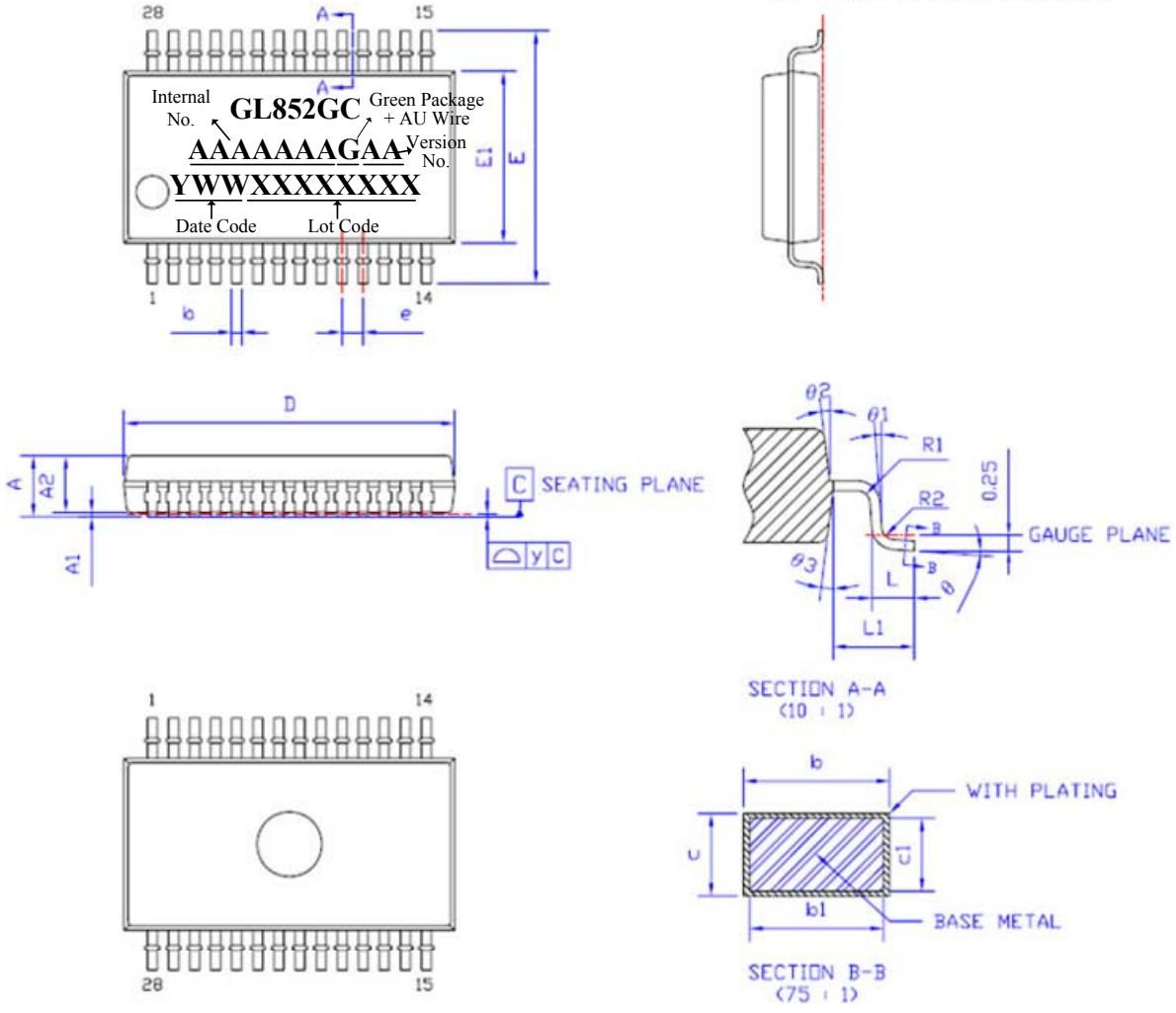


Figure 8.3 - GL852GC 28 Pin SSOP Package

CHAPTER 9 ORDERING INFORMATION

Table 9.1 - Ordering Information

Part Number	Package	Green/Wire Material	Version	Status
GL852GC-MNGXX	LQFP 48	Green Package + AU Wire	XX	Available
GL852GC-OHG*XX	QFN 28	Green Package + AU Wire	XX	Available
GL852GC-HHGXX	SSOP 28	Green Package + AU Wire	XX	Available

*The marking of "OHG" will not be shown on the IC due to QFN 28 package size limitation.