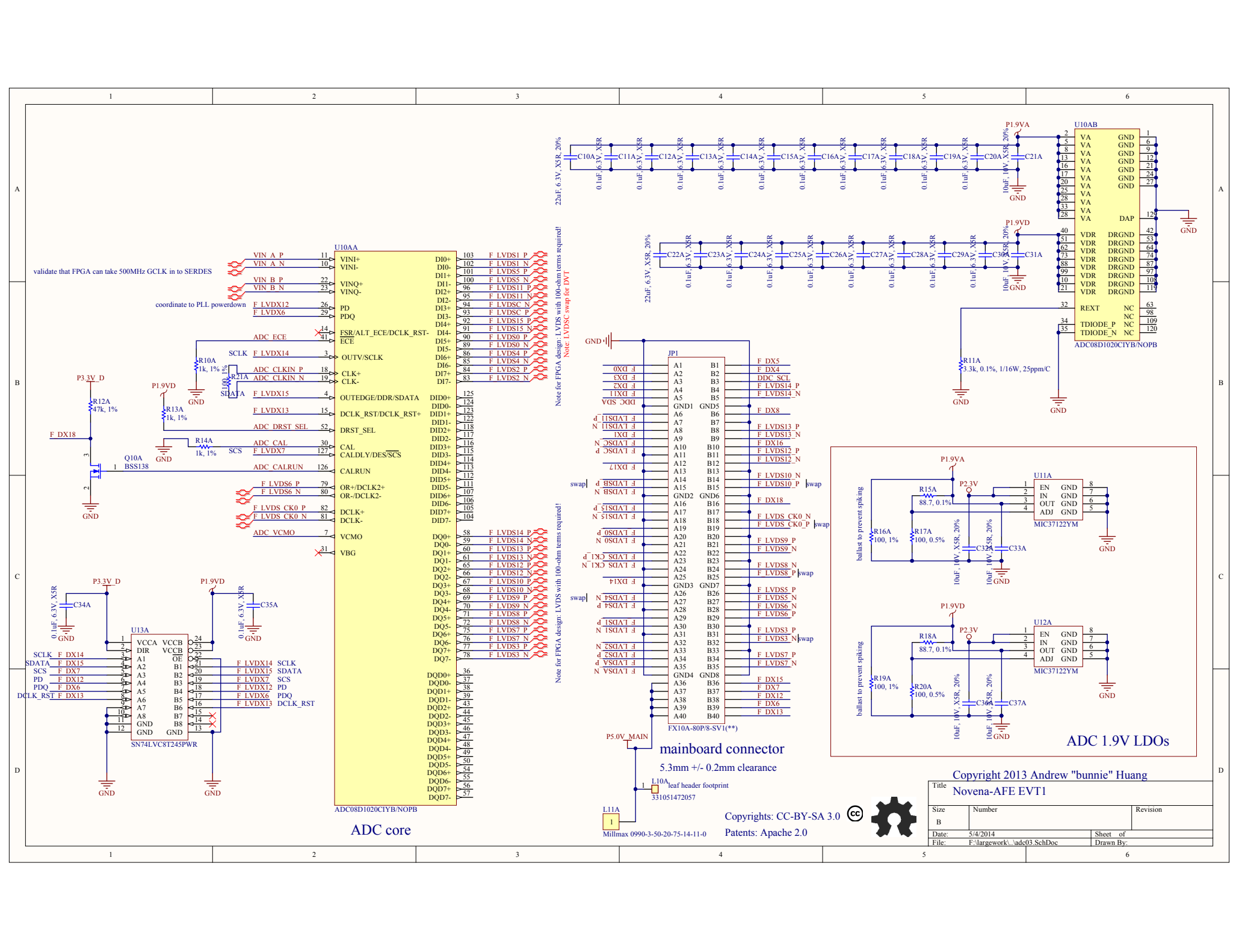
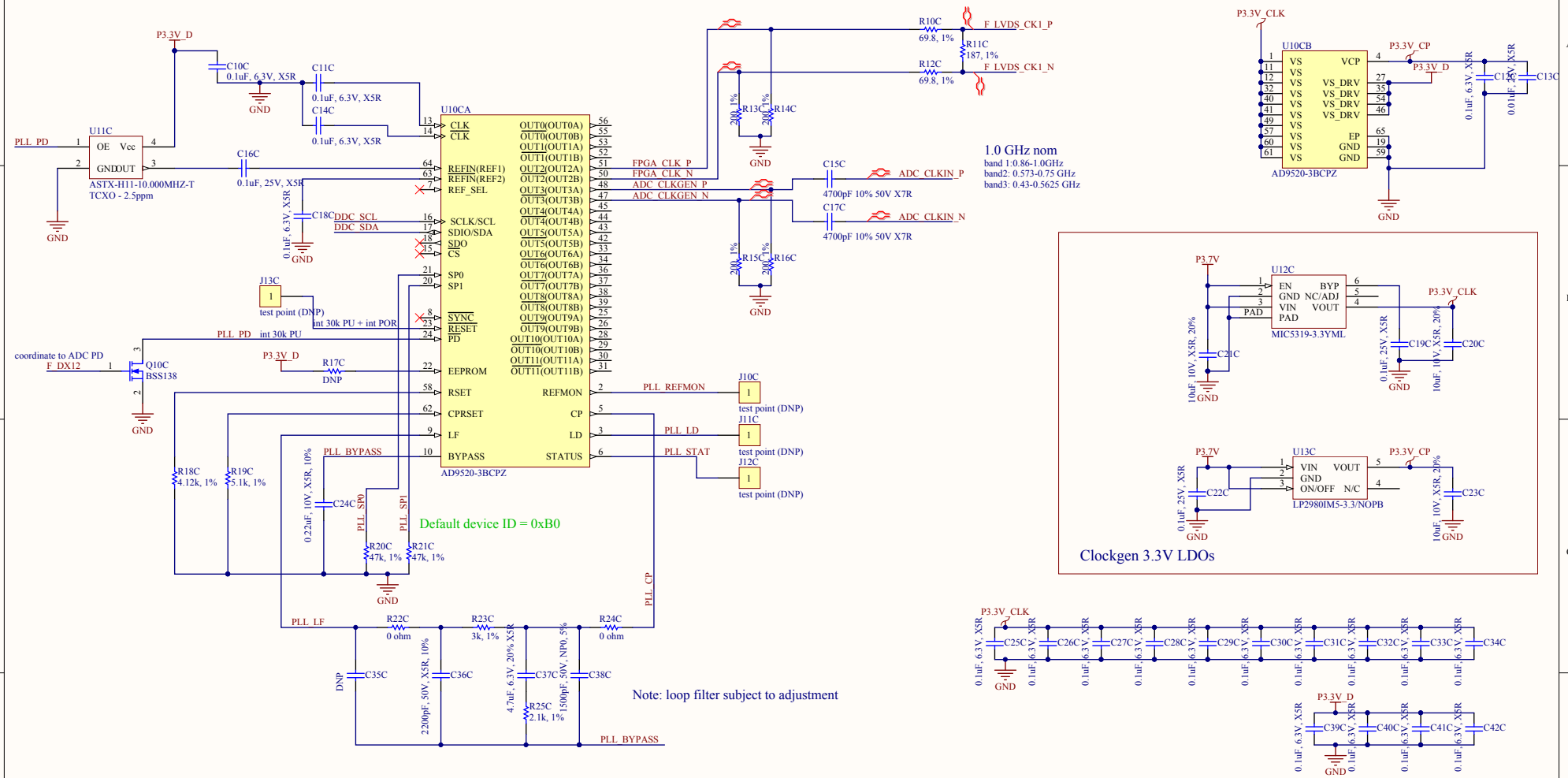
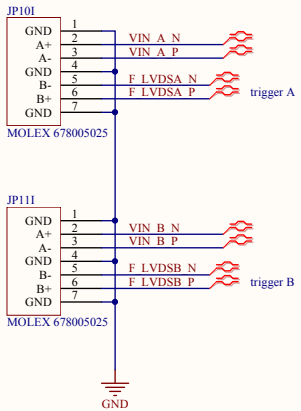

validate that FPGA can take 500MHz GCLK in to SERDES
coordinate to PLL powerdown
Note for FPGA design: LVDS with 100-ohm terms required!
Note: LVDSC swap for DV1
Note for FPGA design: LVDS with 100-ohm terms required!
U10AA
ADC08D1020CIYB/NOPB
ADC core
U10AB
ADC08D1020CIYB/NOPB
U13A
SN74LVC8T245PWR
JP1
FX10A-80P/8-SV1(**)
mainboard connector
5.3mm +/- 0.2mm clearance
leaf header footprint
331051472057
Millmax 0990-3-50-20-75-14-11-0
U11A
MIC37122YM
U12A
MIC37122YM
ADC 1.9V LDOs
ballast to prevent spiking
Copyrights: CC-BY-SA 3.0
Patents: Apache 2.0
Copyright 2013 Andrew "bunnie" Huang
Title
Novena-AFE EVT1
Size
B
Number
Revision
Date: 5/4/2014
Sheet of
File: F:\largework\..\adc03.SchDoc
Drawn By:



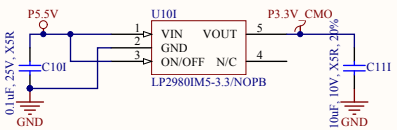


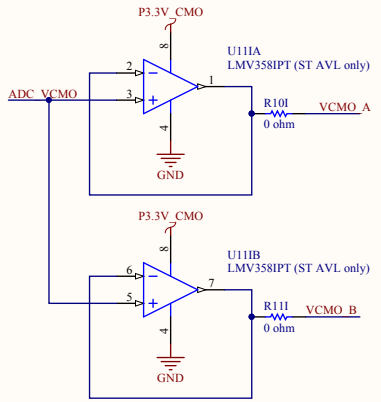

| | | |
|---|---|---|
| Title | Novena-AFE EVT1 | |
| Size: B | Number | Revision |
| Date: 5/4/2014 | Sheet of | |
| File: F:\largework\..\clock02.SchDoc | Drawn By: | |

Use termination plugs to tie unused inputs to VCMO (not GND)

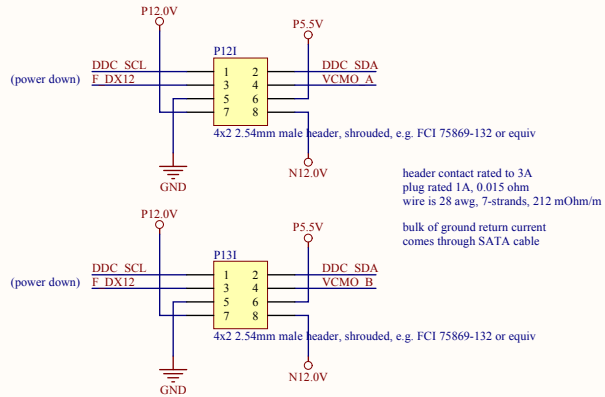



High speed analog signal headers



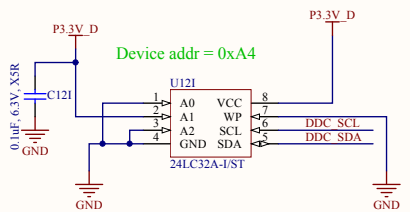

common-mode offset buffers




High speed analog power headers

Rules for connecting (or not connecting) to analog inputs:

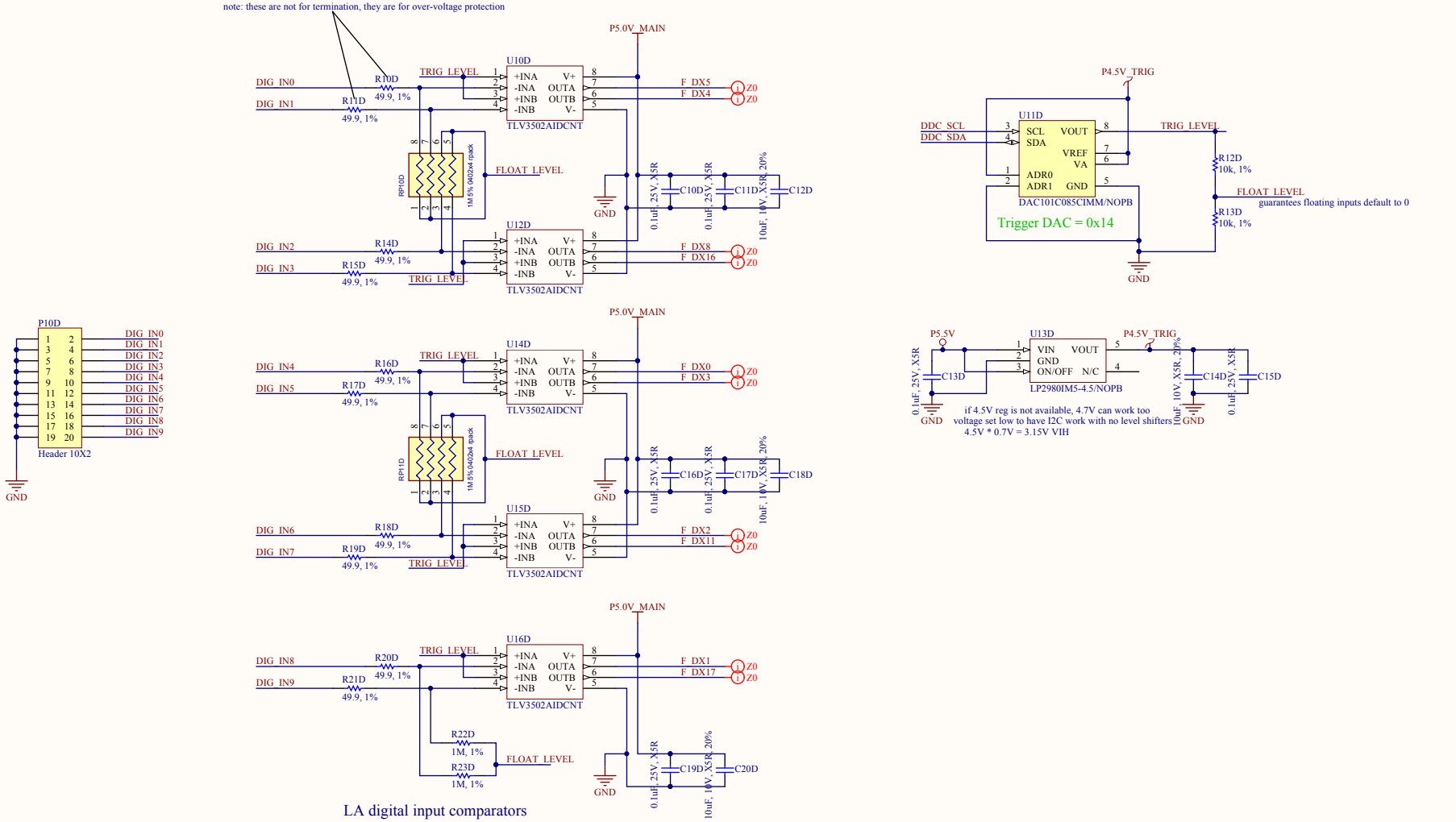
1. If VCMO is supported, it is okay to use DC coupling <-- typ case
2. If AC coupling is used, VCMO must be grounded on the probe side
3. If one channel is AC coupled, and an input pair is unused, tie VCMO to ground, and tie unused inputs to an AC ground (e.g. capacitors to ground)
4. If one channel is DC coupled, and an input pair is unused, tie unused inputs to VCMO directly <-- typ case




ID & cal record EEPROM, 4kx8

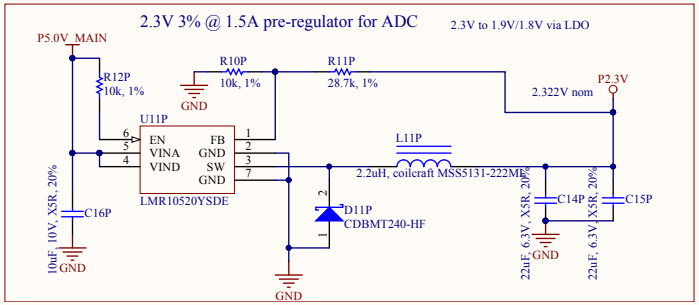


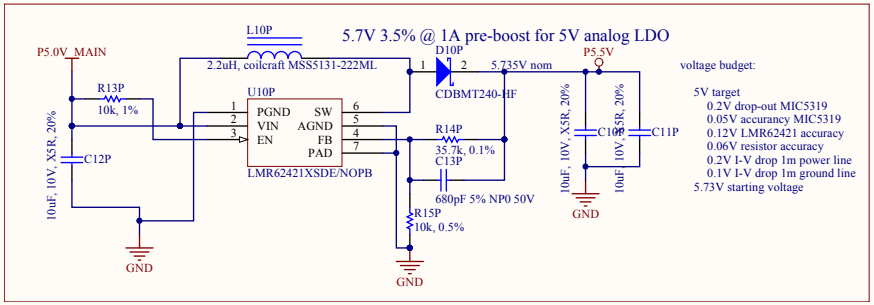
| | | |
|---|---|---|
| Title: Novena-AFE EVT1 | | |
| Size: B | Number | Revision |
| Date: 5/4/2014 | | Sheet of |
| File: F:\largework\..\connect04.SchDoc | | Drawn By: |

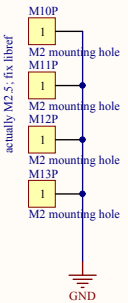


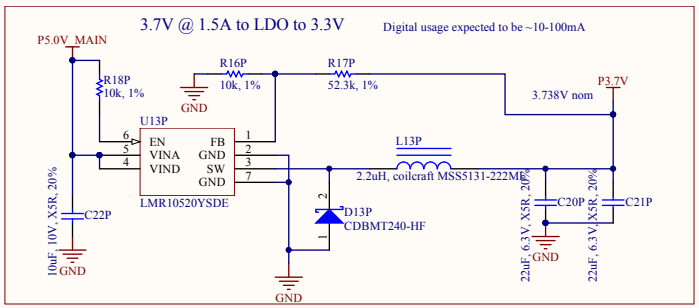


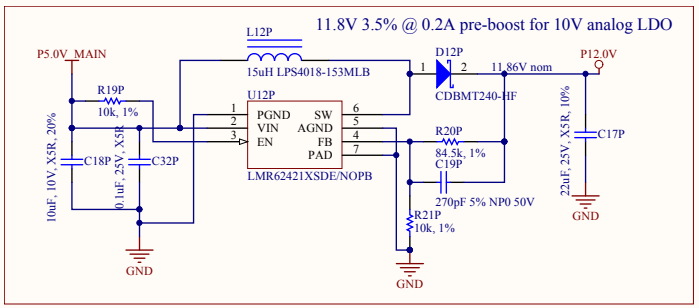

| | | |
|---|---|---|
| Title: Novena-AFE EVT1 | | |
| Size: B | Number | Revision |
| Date: 5/4/2014 | Sheet of | |
| File: F:\largework\..\digital05.SchDoc | Drawn By: | |

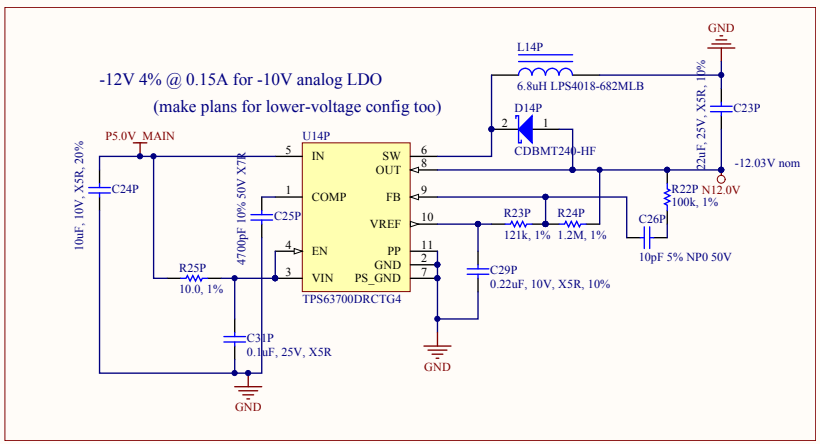


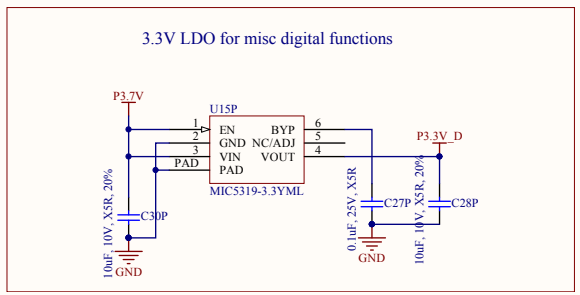




I2C address map:

Trigger DAC = 0x14

ADC EEPROM = 0xA4

Clock generator = 0xB0

Connected on mainboard:
HDMI DDC (0xA0, 0x74, 0x6E, 0x88, 0x94, 0x96)
PMIC (0x10)

(p) Analog Trigger DAC = 0x9A

(p) Probe EEPROM = 0xA6

(p) Analog Trim DAC = 0x9C



| | | |
|---|---|---|
| Title | Novena-AFE EVT1 | |
| Size: B | Number | Revision |
| Date: 5/4/2014 | | Sheet of |
| File: F:\largework\..\power01.SchDoc | | Drawn By: |