Novena PVT2-A

I2C mappings:
addresses are already shifted left by one to accommodate r/w bit
i.e., address is expressed as the write address

I2C: 1.0 pull-up
SMbus functions (optional)
MMA8452 (0x3b) (optional)
SO-DIMM identification (0x3c/3d) (optional)
FPGA (optional)
SO-DIMM temp sensor (0x30) (optional) (optional)
STMP01010 (0x5b) (optional)
Gas gauge and charger via SMB (on battery board)
PCF8523 RTC (0x40)

I2C: 2.0 pull-up
HDMI EDC (0x6a/0x76)
expansion header
FPGA (optional)
PMIC (0x10)

I2C: 3.3V pull-up
LED E2RD (0x69/0x6f)
E2LED (0x63)
FPGA (optional)
Utility EEPROM (0x4A)

Power sequencing

I2C1: 10k pull-up
I2C2: 1.8k pull-up
I2C3: 2.2k pull-up

SMBus functions (optional)
LCD EDID (0xA0)
ES8283 (0x22)
HDMI DDC (0xA0, 0x74)
MMA8452 (0x38) (optional)
SO-DIMM identification (0xA0)
expansion header
FPGA (optional)
Utility EEPROM (0xAC)

SO-DIMM temp sensor (0x30) (optional)
addresses are already shifted left by one to accommodate r/w bit
i.e., address is expressed as the write address

STMPE610 (0x88) (optional)
P1.8V SW4 has option to power VTT
Use this option to lower VTT source to 1.0V to save power

changes on table:
P1.8V VGH31 pin has option to program to 1.0V before using

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Novena PVT2-A

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Internal microSD card (main boot)

External SD card

Utility EEPROM, 64kx8

Note: This document contains the schematic for the Novena PVT2-A development board. It includes various components and connections, such as microSD card interfaces, SD card slots, and other electronic components. The diagram is designed to help developers understand the internal architecture and connectivity of the board.

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SATA connector arrangement

uses M-F extender combo cables

For boot: compatible ONLY with SATA-II (3Gbps) drives
Optimized for use with SSDs

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Novena PVT2-A
i.MX6 S/DL has AUD_MCLK on P4

 UART4_RXD

 0.1uF, 6.3V, X5R

 4.7uF, 10V, X5R, 10%

 100k, 1%

 15k, 1%

 10k, 1%

 Also means BATT_PWR > 6V to turn-on transistor

 Can’t use 2N7002 here b/c Vth is too high

 Matched Net Lengths [Tolerance = 40mil]

 Requires custom cable to adapt pinout to specific LCD

 Requires custom cable to adapt pinout to specific LCD

 Voltage range compatible with most LED backlit displays

 Capacitor placement and decoupling not critical

 No leakage point on 3.3V line

 Inrush current limit is 200mA

 Internal pull-down resistors on 3.3V power rail

 1.0uF, 25V, 20% X5R

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 HDMI ESD


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 Novena PVT2-A
When apoptosis is high, resetting the FPGA resets the CPU.