Novena PVT2-A

Power sequencing

rail name	voltage	dependent blocks	sheet	derived from	sequence	generated by	capacity	notes
RAW_PWR	7V-17V	5V maxter	05pwr_input	external	0	AC adapter	3A	when using only AC adapter, 12V nominal
BATT_PWR	6V-18V	5V maxter	05pwr_input	external external	0 0	AC adapter battery pack	3A – 6A	3- and 4- cell Li-Ion are preferred configurations
P5.0V	5V	3.3V maxter VTT regulator	05pwr_input	BATT_PWR	1	NCP30208	7A	
P5.0V_DELAYED	5V	SATA connector USB ports USB hub (maxter & slave) * USB_OTG_VBUS HDMI 5V Speaker amplifier PWM I/O block (option) ADC 3.3V regulator expandion header	05pwr_input	P5.0V	6	SI4435DY	7A	delay control is P2.5V_VGEN5 to power unused 3.3V regulator circuit
P3.3V	3.3V	DDR3 SO-DIMM PMIC VIN3 PMIC SW inputs Battery interface voltages MCU Reset	05pwr_input	P5.0V	1	FAN53540UCX	5A	
P3.3V_DELAYED	3.3V	NVCC_LCD NVCC_GPIO NVCC_SD1, 2 and 3 NVCC_NANDF NVCC_JTAG NVCC_EIM0, 1, and 2 PMIC_VIN2 Boot config straps JTAG internal MicroSD pawitch external SD card utility EEPROM USB hub (maxter & slave) SATA connector 100Mbit ethernet PCIE pawitch LCD panel digital microphone audio codec pawitch FPGA I/O FPGA expansion I/O Apoptosis circuit FPGA serial memories accelerometer expansion header UART 3;4 headers via schottky	05pwr_input	P3.3V	6	SI4435DY	5A	delay control is P2.8V_VGEN6 actual voltage closer to 2.9V/3.0V

rail name	voltage	dependent blocks	sheet	derived from	sequence	generated by	capacity	notes
VCC_1.2V_SW1AB	1.35V	VDDARM_IN, VDDARM23_IN	02cpu_power	P3.3V	3	PMIC	2.5A	draft at 1.375V
VDD_SOC_IN_SW1C	1.225V	VDDSOC_IN	02cpu_power	P3.3V	3	PMIC	1.75A	draft at 1.375V
P3.0V_VDDHIGH_SW2	3.0V	VDDHIGH_IN VIN1 of PMIC	02cpu_power	P3.3V	4	PMIC	2A	virtually unused
P1.5V_DDR_SW3	1.5V	DDR3 on SoC DDR3 SO-DIMM VTT regulator reference			5	PMIC	2.5A	
P1.8V_SW4	1.8V		04pwr_amic	P3.3V	5	PMIC	1A	unused!
P5.0V_SWBST	5V		04pwr_amic	P3.3V	soft	PMIC	0.5A	unused!
P1.2V_VGEN1	1.2V		04pwr_amic	P3.0V_VDDHIGH_SW2	soft	PMIC	0.1A	unused!
P1.5V_VGEN2	1.5V	PCI-express	04pwr_amic	P3.0V_VDDHIGH_SW2	4	PMIC	0.25A	note PCIE spec is 0.375A
P1.8V_VGEN3	??		04pwr_amic	P3.3V_DELAYED	soft	PMIC	0.1A	1.8V by BSP, soft startup sequenced
P1.8V_VGEN4	1.8V		04pwr_amic	P3.3V_DELAYED	5	PMIC	0.35A	unused!
P2.5V_VGEN5	2.5V	Power-on LED P5.0V_DELAYED control RGMII I/O NVCC_ENET NVCC_RGMII NVCC_CSI	04pwr_amic	P3.3V	5	PMIC	0.1A	1.5mA to LED 37 mA to PHY
P2.8V_VGEN6	2.8V	P2.8V_DELAYED control	04pwr_amic	P3.3V	5	PMIC	0.2A	
P3.3V_LICELL	2.5-3.3V	0.06F supercap P3.0V_STBY	04pwr_amic	P3.3V	1	PMIC	0.00006A	?? override 2.5V default to 3.3V
P3.0V_STBY	3.0V	CPU boot pins	04pwr_amic	P3.3V & P3.3V_LICELL	2	PMIC	0.0004A	(VSNVS)
P0.75V_REFDDR	0.75V	VTT regulator	02cpu_sodimm	P1.5V_DDR_SW3	5	PMIC	0.015A	
P0.75V_DDR3_VTT	0.75V	DDR3 SO-DIMM	02cpu_sodimm	P5.0V	6	RT9045GSP	1.5A	controlled by P0.75V_DDR3_VTT
SDCARD_VDD	3.3V	microSD card	07sdcard	P3.3V_DELAYED	soft	FDN304P	0.2A	controlled by SD3_RST
EN1G_P1.2V	1.2V	Gigabit ethernet	11ethernet90bit	P5.0V	soft	LMR10510YSD	1A	delay control is P3.3V_DELAYED
EN1G_P1.2VA	1.2V	Gigabit ethernet	11ethernet90bit	EN1G_P1.2V	soft	Ferrite bead	1A	
EN1G_3.3VA	3.3V	Gigabit ethernet	11ethernet90bit	P3.3V_DELAYED	5	Ferrite bead		
P5.0V_SATA	5V	SATA connector	09sata	P5.0V_DELAYED	soft	SI4435DY	2A	SATA_PWRON manual control
EN100_A3.3V	3.3V	100Mbit ethernet	10ethernet100	P3.3V_DELAYED	5	Ferrite bead	0.5A	
EN100_D1.8V	1.8V	100Mbit ethernet	10ethernet100	P3.3V_DELAYED	5	AXIB772B		
EN100_A1.8V	1.8V	100Mbit ethernet	10ethernet100	P3.3V_DELAYED	5	Ferrite bead		
MPCIE_3.3V	3.3V	PCI-express	12mPCIe	P3.3V_DELAYED	soft	FDN304P	1A	PCIE_PWRON manual control
SIM_PWR	3.3V	SIM	12mPCIe	P3.3V_DELAYED	soft	FDN304P	0.1A	SIM_PWRON control; beware conflict with mPCIE sourcing
TX_HDMI_5V	5V	HDMI	13hdmi_lcd	P5.0V_DELAYED	5	50mA fuse	0.05A	
LCD_VCC_SW	3.3V	LCD panel	13hdmi_lcd	P3.3V_DELAYED	soft	SI4435DY	2A	LCD_PWR_CTL; note active pulldown during power-off
LCD_BL_VDD	5V-18V	LCD backlight	13hdmi_lcd	BATT_PWR	soft	SI4435DY	2A	LCD_PWR_CTL for master power cutoff
AUD_P3.3V	3.3V	audio codec	14audio	P3.3V_DELAYED	soft	FDN304P	0.5A	AUD_PWRON; note active pulldown during power-off
P1.2V	1.2V	FPGA core	15fpga	P5.0V_DELAYED	6	LMR10510YSD	1A	always on
VANA	3.3V	ADC	15fpga	P5.0V_DELAYED	6	LP2980IM5-3.3	0.05A	always on

rail name	voltage	dependent blocks	sheet	derived from	sequence	generated by	capacity	notes
P5.0V_WIFI	5V	USB wifi option	08usb	P5.0V_DELAYED	soft	RT9706	0.5A	USB_PWREN3_N off of main hub
P5.0V_USBEXT1	5V	external USB	08usb	P5.0V_DELAYED	soft	RT9711B0B	1.5A	USB_PWREN1_N off of main hub
P5.0V_USBEXT2	5V	external USB	08usb	P5.0V_DELAYED	soft	RT9711B0B	1.5A	USB_PWREN5_N off of slave hub
P5.0V_MOUSE	5V	mouse	08usb	P5.0V_DELAYED	soft	RT9706	0.5A	USB_PWREN7_N off of slave hub
P5.0V_KB0	5V	keyboard	08usb	P5.0V_DELAYED	soft	RT9706	0.5A	USB_PWREN8_N off of slave hub
USB_VID_P5V	5V	video camera	13hdmi_lcd	P5.0V_DELAYED	soft	RT9706	0.5A	USB_PWREN6_N off of slave hub

I2C mappings:

addresses are already shifted left by one to accommodate r/w bit
i.e., address is expressed as the write address

I2C1: 10k pull-up
- SMBus functions (optional)
- MMA8452 (0x38) (optional)
- SO-DIMM identification (0xA0)
- FPGA (optional)
- SO-DIMM temp sensor (0x30) (optional)
- STMPE610 (0x88) (optional)
- Gas gauge and charger via SMB (on battery board)
- PCF8523 RTC (0xD0)

I2C2: 1.8k pull-up
- HDMI DDC (0xA0, 0x74)
- expansion header
- FPGA (optional)
- PMIC (0x10)

I2C3: 2.2k pull-up
- LCD EDID (0xA0)
- ES8283 (0x22)
- FPGA (optional)
- Utility EEPROM (0xAC)

P1.8V_SW4 has option to power VTT
Use this option to lower VTT source to 1.0V to save power

changes on table:

P1.8V_VGEN3 micbias gen option
(reprogram to 3.0V before using)

U_02cpu_power
02cpu_power.SchDoc

U_06cpu_soc
06cpu_soc.SchDoc

U_10ethernet100
10ethernet100.SchDoc

U_14audio
14audio.SchDoc

U_03cpu_sodimm
03cpu_sodimm.SchDoc

U_07sdcard
07sdcard.SchDoc

U_11ethernetGbit
11ethernetGbit.SchDoc

U_15fpga
15fpga.SchDoc

U_04pwr_pmic
04pwr_pmic.SchDoc

U_08usb
08usb.SchDoc

U_12mPCIe
12mPCIe.SchDoc

U_16gpio_misc
16gpio_misc.SchDoc

U_05pwr_input
05pwr_input.SchDoc

U_09sata
09sata.SchDoc

U_13hdmi_lcd
13hdmi_lcd.SchDoc

NTLOGO

Novena Logo

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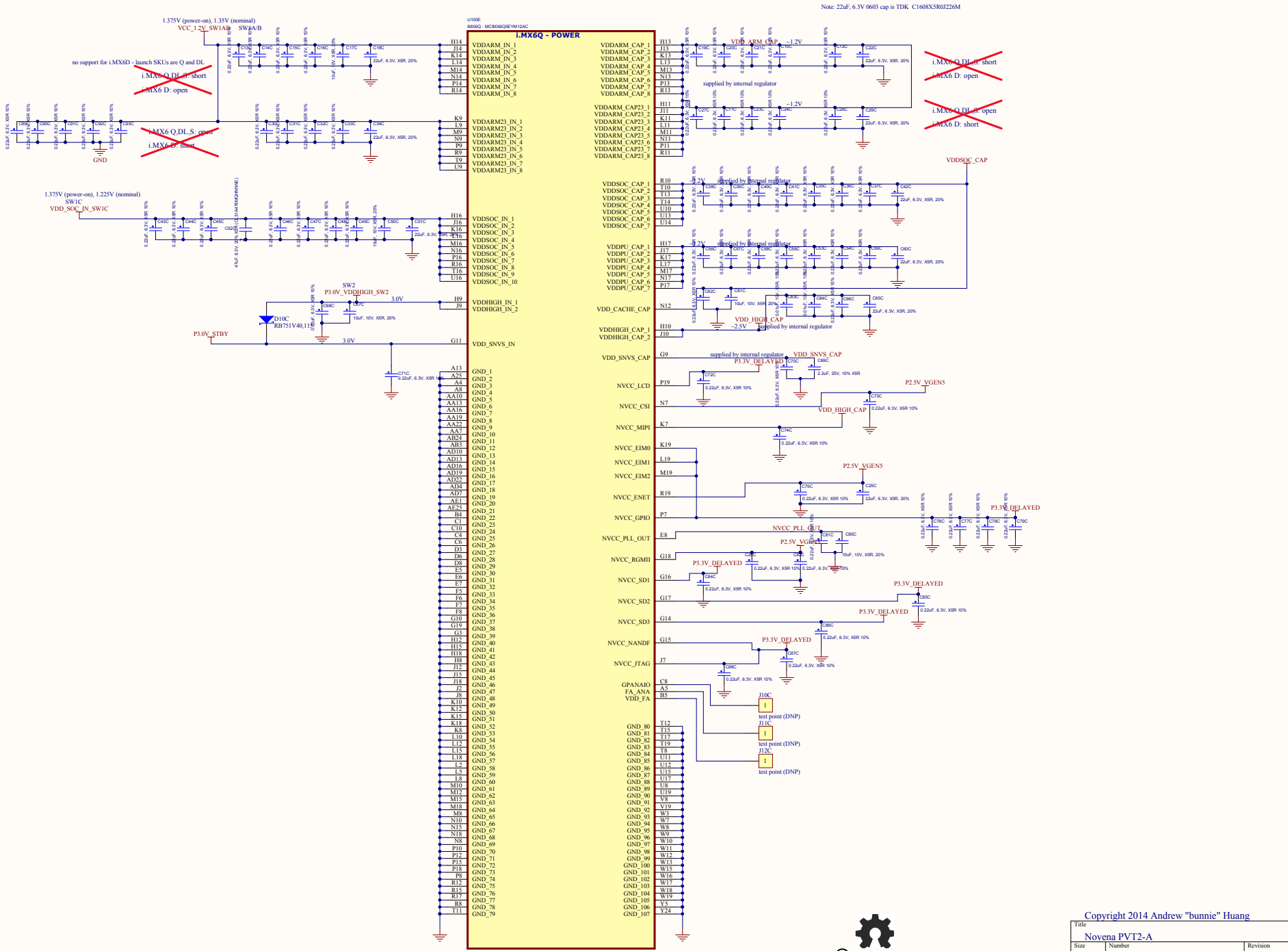
i.MX6Q - POWER
Note: 22uF, 6.3V 0603 cap is TDK C1608X5R0J226M
1.375V (power-on), 1.35V (nominal)
VCC_1.2V_SW1AB
SW1A/B
no support for i.MX6D - launch SKUs are Q and DL
i.MX6 Q,DL,S: short
i.MX6 D: open
i.MX6 Q,DL,S: open
i.MX6 D: short
GND
1.375V (power-on), 1.225V (nominal)
SW1C
VDD_SOC_IN_SW1C
SW2
P3.0V_VDDHIGH_SW2
3.0V
D10C
RB751V40,115
P3.0V_STBY
VDDARM_CAP
~1.2V
supplied by internal regulator
VDDSOC_CAP
VDDPU_CAP
VDD_HIGH_CAP
~2.5V
VDD_SNVS_CAP
P3.3V_DELAYED
P2.5V_VGEN5
NVCC_PLL_OUT
test point (DNP)
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Novena PVT2-A
Size C
Number
Revision
Date: 7/8/2014
Sheet of
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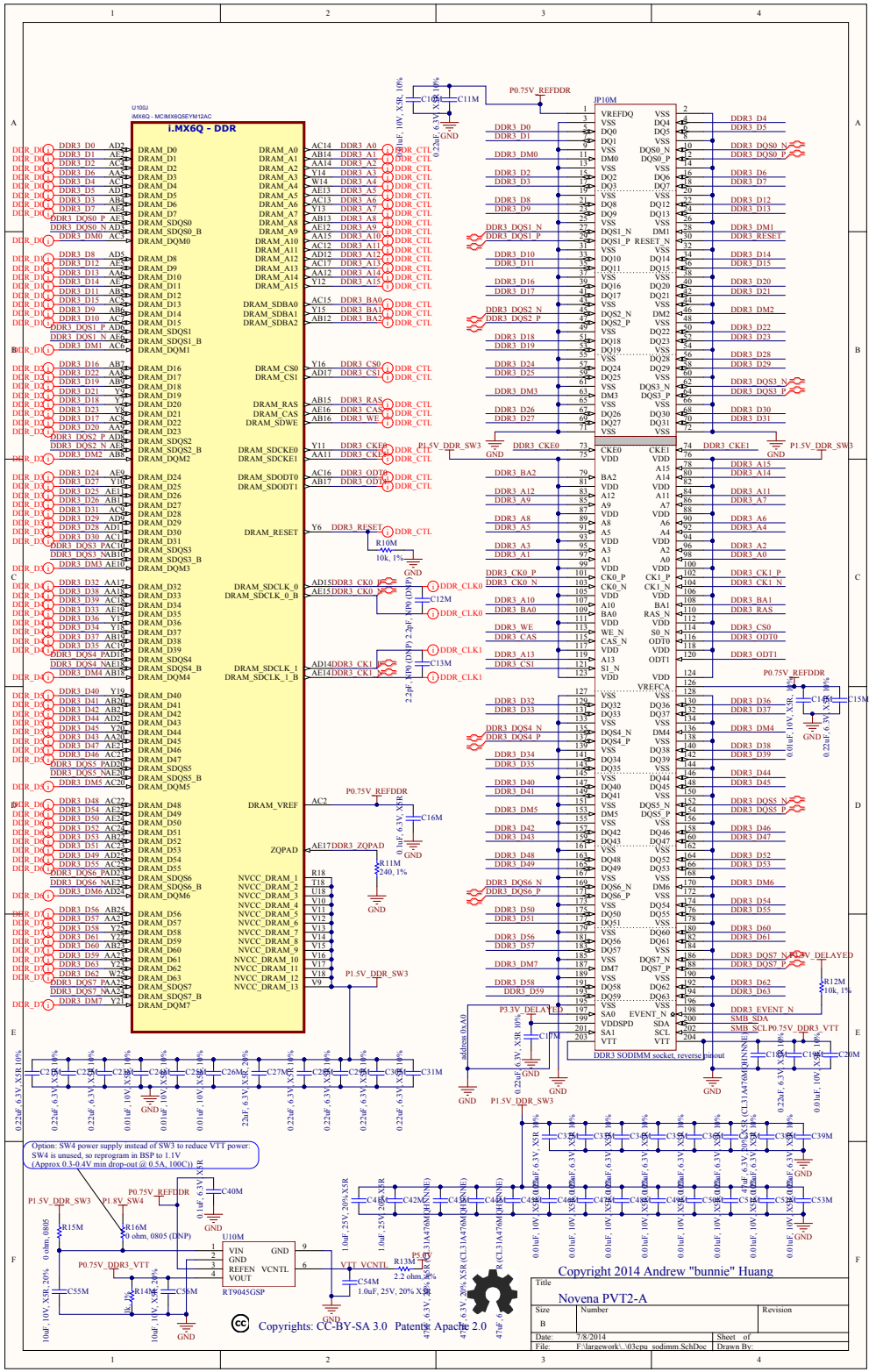
Drawn By:


i.MX6Q - DDR
JP10M
DDR3 SODIMM socket, reverse pinout
P0.75V_REFDDR
P1.5V_DDR_SW3
P3.3V_DELAYED
P0.75V_DDR_VTT
P1.8V_SW4
U10M
RT9045GSP
Option: SW4 power supply instead of SW3 to reduce VTT power:
SW4 is unused, so reprogram in BSP to 1.1V
(Approx 0.3-0.4V min drop-out @ 0.5A, 100C))
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Novena PVT2-A
Size B
Number
Revision
Date: 7/8/2014
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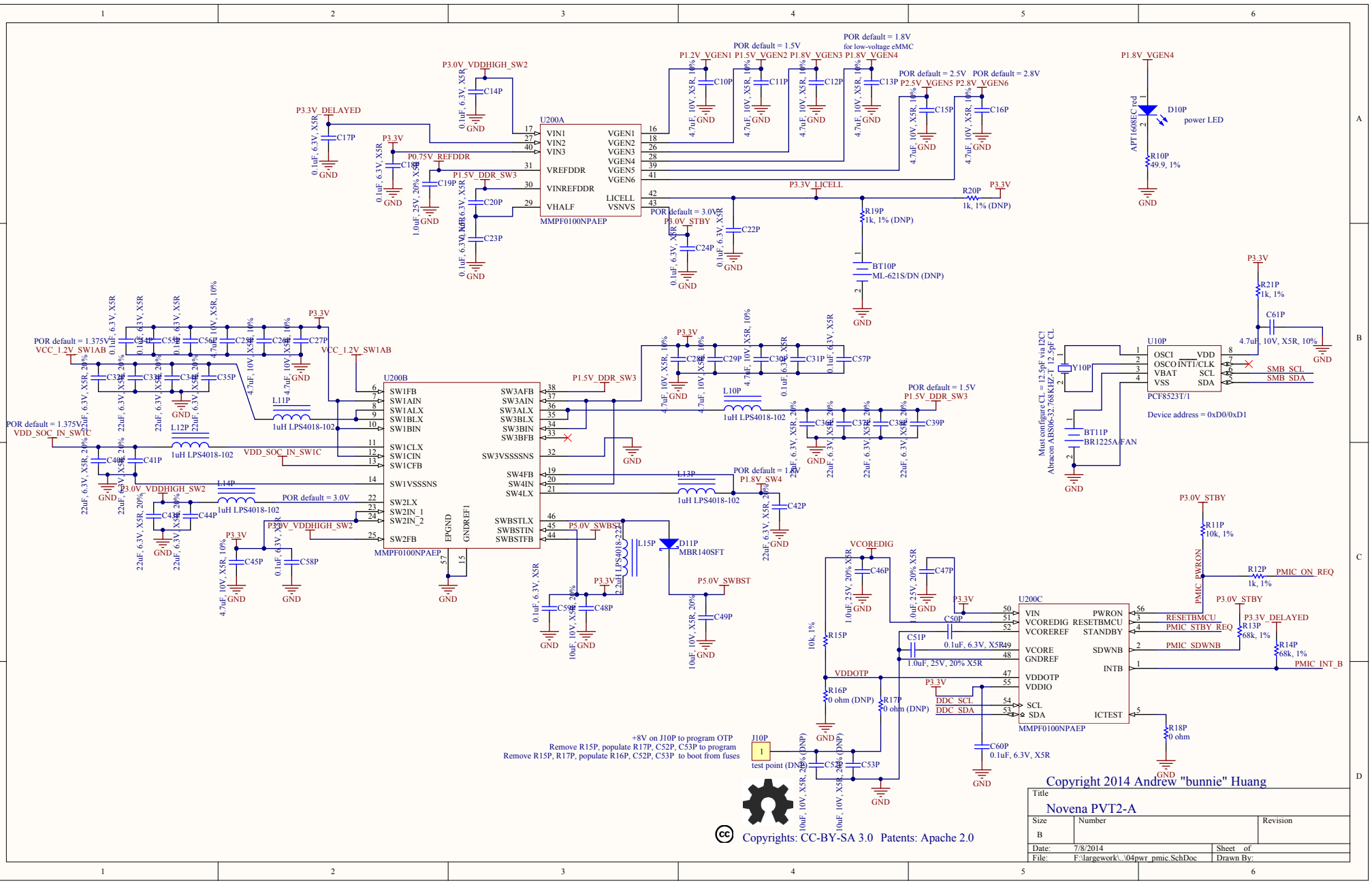

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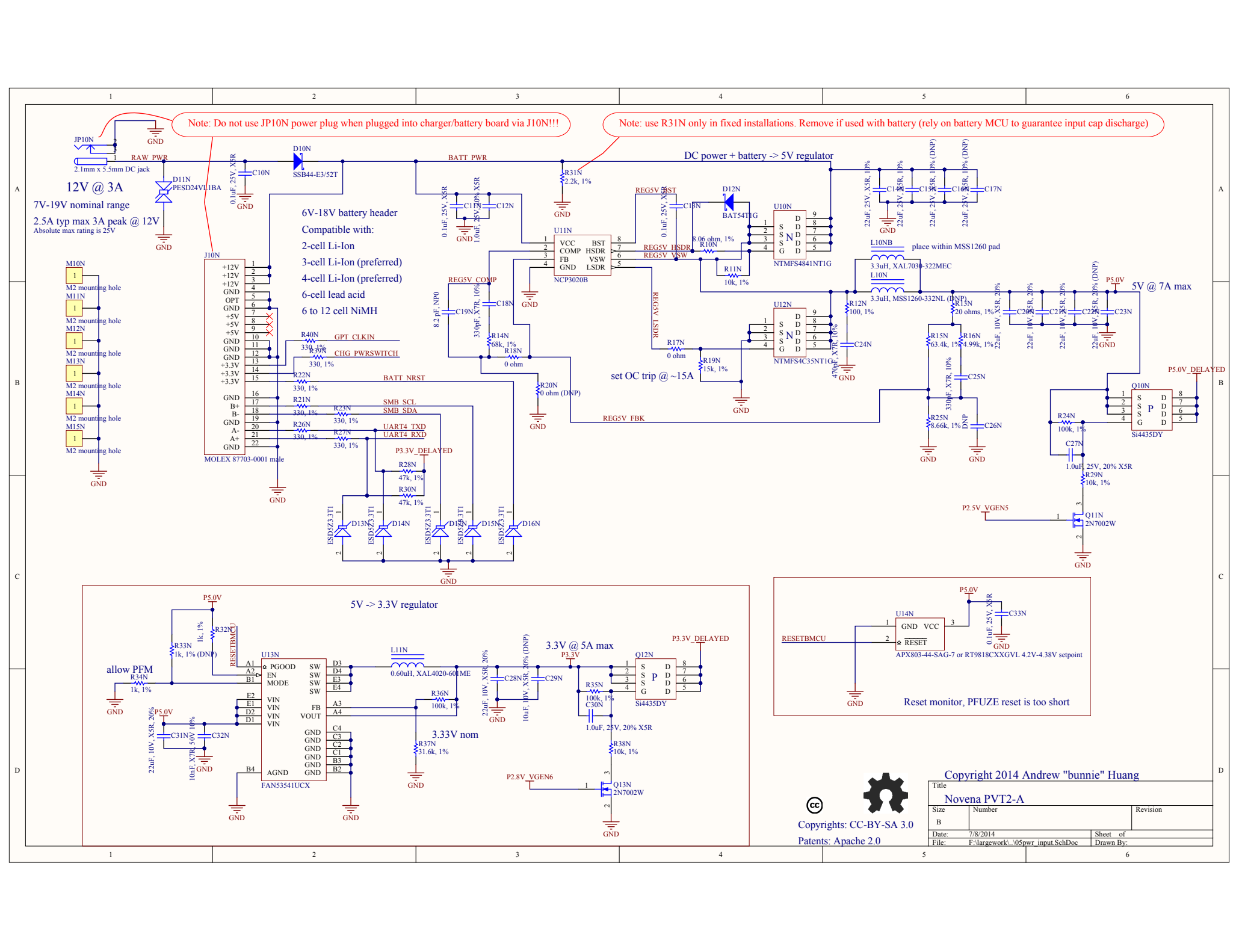
Note: Do not use JP10N power plug when plugged into charger/battery board via J10N!!!
Note: use R31N only in fixed installations. Remove if used with battery (rely on battery MCU to guarantee input cap discharge)
DC power + battery -> 5V regulator
12V @ 3A
7V-19V nominal range
2.5A typ max 3A peak @ 12V
Absolute max rating is 25V
6V-18V battery header
Compatible with:
2-cell Li-Ion
3-cell Li-Ion (preferred)
4-cell Li-Ion (preferred)
6-cell lead acid
6 to 12 cell NiMH
5V @ 7A max
set OC trip @ ~15A
5V -> 3.3V regulator
3.3V @ 5A max
3.3V nom
allow PFM
Reset monitor, PFUZE reset is too short
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Novena PVT2-A

A, B, and C correspond to labelled jumpers below

	BT_MD		BT_CFG1								BT_CFG2							
Bit position	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Common bits			0			0/PU	0	0		0	0	0	1			0	0	0
serial vs. normal	A	A																
SD vs. SATA				B	B													
SD int. v ext									C					C	C			

P_TAMPER
Male 2.54mm 2x1 right angle (DNP)

hard reset
TL3342F160QG/TR
SW10B
P3.3V
R17B 10k, 1%
C10B 0.1uF, 25V, X5R (DNP)
GND

TL3342F160QG/TR (DNP)
SW11B
DNP; CPU power state controlled by charger board
GND

NT10B
Heat sink Advanced Thermal Solutions ATS-56001-C3-R0

U100A
iMX6Q - MCIMX6Q5EYM12AC
i.MX6Q - EIM

EIM_LBA	K22	EIM_LBA
EIM_OE	J24	EIM_OE
EIM_RW	K20	EIM_RW
EIM_CS0	H24	EIM_CS0
EIM_CS1	J23	EIM_CS1
EIM_A16	H25	EIM_A16
EIM_A17	G24	EIM_A17
EIM_A18	J22	EIM_A18
EIM_A19	G25	UIM_DATA
EIM_A20	H22	UIM_CLK
EIM_A21	H23	UIM_RESET
EIM_A22	F24	PCIE_WDIS_N
EIM_A23	F21	UIM_PWRON
EIM_A24	F25	HDMI_HPD_CPU
EIM_A25	H19	CEC
EIM_D16	C25	DDC_SDA
EIM_D17	F21	I2C3_SCL
EIM_D18	D24	I2C3_SDA
EIM_D19	G21	EPIT1_EPITO
EIM_D20	G20	EPIT2_EPITO
EIM_D21	H20	SMB_SCL
EIM_D22	E23	PCIE_WAKE
EIM_D23	D25	RGMII_NRST
EIM_D24	F22	UART3_TXD
EIM_D25	G22	UART3_RXD
EIM_D26	E24	UART2_TXD
EIM_D27	E25	UART2_RXD
EIM_D28	G23	SMB_SDA
EIM_D29	J19	PCIE_RST
EIM_D30	J20	SATA_PWRON
EIM_D31	H21	
EIM_EB2	F22	DDC_SCL
EIM_EB3	F23	
EIM_BCLK	N22	EIM_BCLK
EIM_WAIT	M25	EIM_WAIT
EIM_EB0	K21	
EIM_EB1	K23	
EIM_DA0	L20	EIM_DA0
EIM_DA1	J25	EIM_DA1
EIM_DA2	J21	EIM_DA2
EIM_DA3	K24	EIM_DA3
EIM_DA4	L22	EIM_DA4
EIM_DA5	L23	EIM_DA5
EIM_DA6	K25	EIM_DA6
EIM_DA7	L25	EIM_DA7
EIM_DA8	L24	EIM_DA8
EIM_DA9	M21	EIM_DA9
EIM_DA10	M22	EIM_DA10
EIM_DA11	M20	EIM_DA11
EIM_DA12	M24	EIM_DA12
EIM_DA13	M23	EIM_DA13
EIM_DA14	N23	EIM_DA14
EIM_DA15	N24	EIM_DA15

BT_CFG1_0 … BT_CFG2_7

Note: SMB pins on this sheet are only used for D/Q config

P3.3V
R23B 10k, 1% (DNP)
P_USB
A
2 pin 1.27mm male header
R25B 10k, 1%
R27B 100k, 1%
R28B 10k, 1%
Q10B 2N7002W
R29B 10k, 1%
header absent = boot from storage
header present = boot from USB
0 = disable tamper detect
P_FUSE
2 pin 1.27mm male header

Y10B
24.0000 MHz 15ppm 8pF 70 ohm ESR (NDK NX3225SA)
R32B 10M, 1% (DNP)
R33B 2.2M, 1%
C11B 18pF, NP0
C12B 18pF, NP0

Abracon ABS06-32.768KHZ-T 12.5pF CL
Y11B
C13B 18pF, NP0
C14B 18pF, NP0
R34B 10M, 1% (DNP)

U100C
iMX6Q - MCIMX6Q5EYM12AC
i.MX6Q - CONTROL

CPU_ONOFF	D12	ONOFF
RESETBMCU	C11	POR_B
CPU_BOOTMODE0	C12	BOOT_MODE0
CPU_BOOTMODE1	F12	BOOT_MODE1
CPU_TEST_MODE	E12	TEST_MODE
CPU_TAMPER	E11	TAMPER
PMIC_STBY_REQ	F11	PMIC_STBY_REQ
PMIC_ON_REQ	D11	PMIC_ON_REQ
CPU_XTALI	A7	XTALI
CPU_XTALO	B7	XTALO
RTC_XTALI	D9	RTC_XTALI
RTC_XTALO	C9	RTC_XTALO

JTAG_TCK	H5	JTAG_TCK
JTAG_TMS	C3	JTAG_TMS
JTAG_TDI	G5	JTAG_TDI
JTAG_TDO	G6	JTAG_TDO
JTAG_TRSTB	C2	JTAG_TRSTB
JTAG_MOD	H6	JTAG_MOD
CLK1_N	C7	CLK1_N
CLK1_P	D7	CLK1_P
CLK2_N	C5	CLK2_N
CLK2_P	D5	CLK2_P

P3.3V_DELAYED
R14B 10k, 1%
R15B 10k, 1%
R16B 10k, 1%
R13B 100, 1%
P10B
Male 2.54mm 8x2 header (DNP)
JTAG_JRST
JTAG_JTDI
JTAG_JTMS
JTAG_JTCK
JTAG_RTCK
JTAG_JTDO
JTAG_NRST
RESETBMCU R18B 0 ohm
R19B 10k, 1%
R20B 1k, 1%
R22B 10k, 1% (DNP)
R26B 4.7k, 1%
GND

PCIE_CLK
PCIE_REFCLK_N
PCIE_REFCLK_P
PCIE_CLK
R57B 100, 1% (DNP)

P3.3V_DELAYED
R35B 10k, 1%
R36B 0 ohm (DNP)
R37B 4.7k, 1%
R38B 4.7k, 1%
R40B 4.7k, 1%
R42B 4.7k, 1%
R44B 4.7k, 1%
BT_CFG1_1
BT_CFG1_5
BT_CFG1_6
BT_CFG2_3
BT_CFG2_4

R46B 10k, 1%
R47B 10k, 1%
R48B 10k, 1%
R49B 10k, 1%
R50B 10k, 1%
R51B 10k, 1%
R52B 10k, 1%
R53B 10k, 1%
R54B 10k, 1%
R55B 10k, 1%
GND

BOOT_CFG1[7:0]: 0XX0 00X0
BOOT_CFG2[7:0]: 001X X000

P3.3V_DELAYED
P_SATA
B
2 pin 1.27mm male header
R43B 10k, 1%
Q13B 2N7002W
header absent = boot from SD
header present = boot from SATA
R56B 10k, 1%
BT_CFG1_6 = !BT_CFG1_5

P3.3V_DELAYED
P_EXT
C
2 pin 1.27mm male header
R41B 10k, 1%
R39B 10k, 1%
BT_CFG1_1 <- replicate to isolate -> BT_CFG2_4
Q11B 2N7002W
Q12B 2N7002W
R45B 10k, 1%
header absent = boot from internal SD
header present = boot from external SD
BT_CFG1_1 = !BT_CFG2_3
BT_CFG2_4 = !BT_CFG2_3

Default boot: internal microSD
Boot select header precedence: P_USB (A) > P_SATA (B) > PEXT (C)
P_FUSE must be used alone, if at all

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Size	B	Number	Revision
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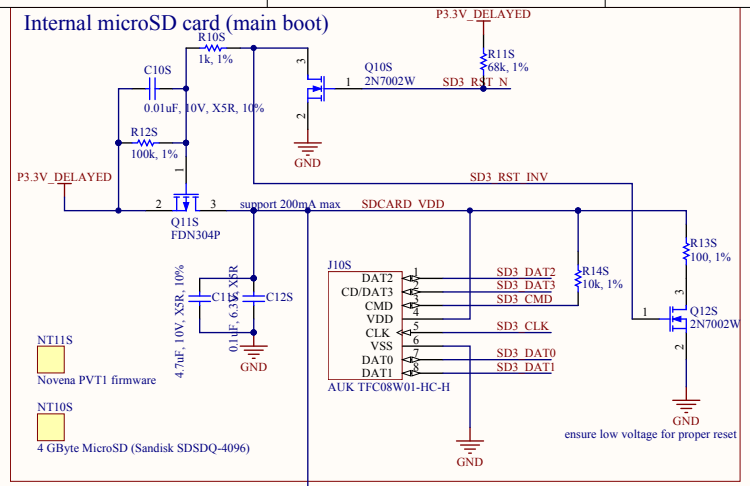

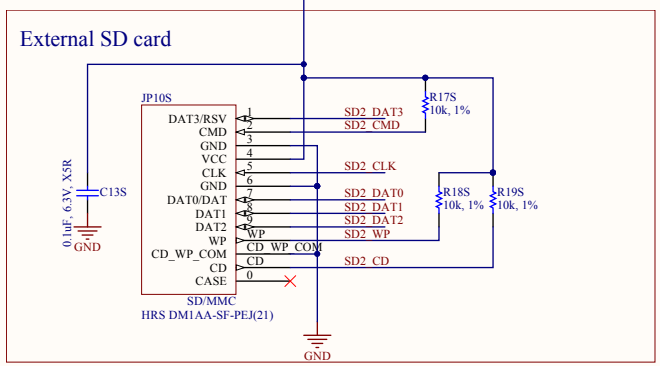

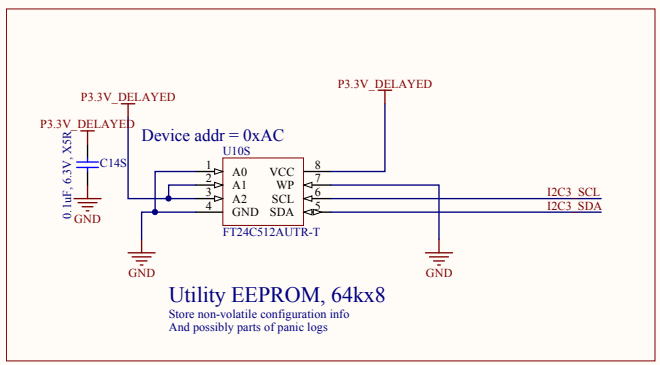

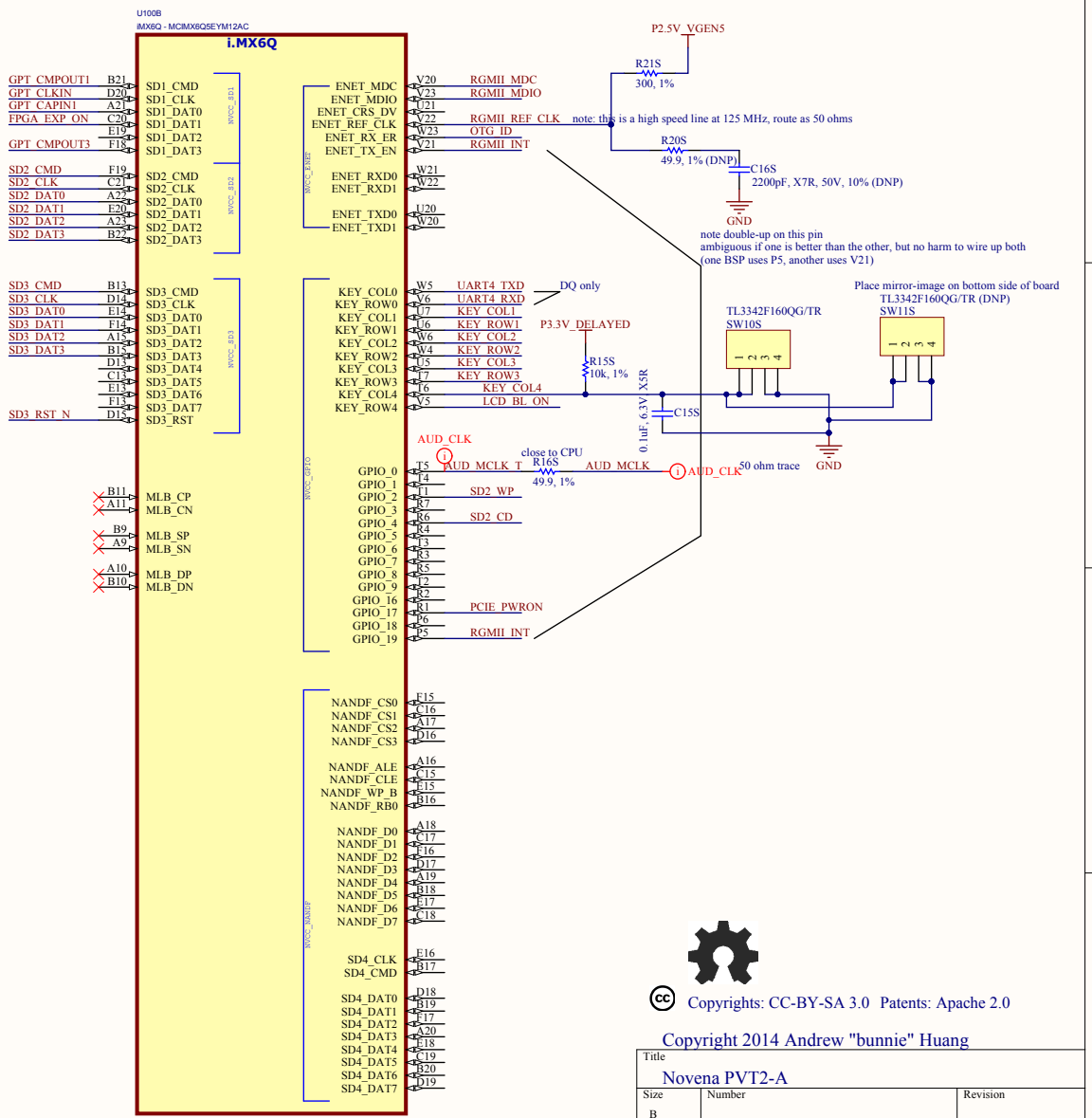

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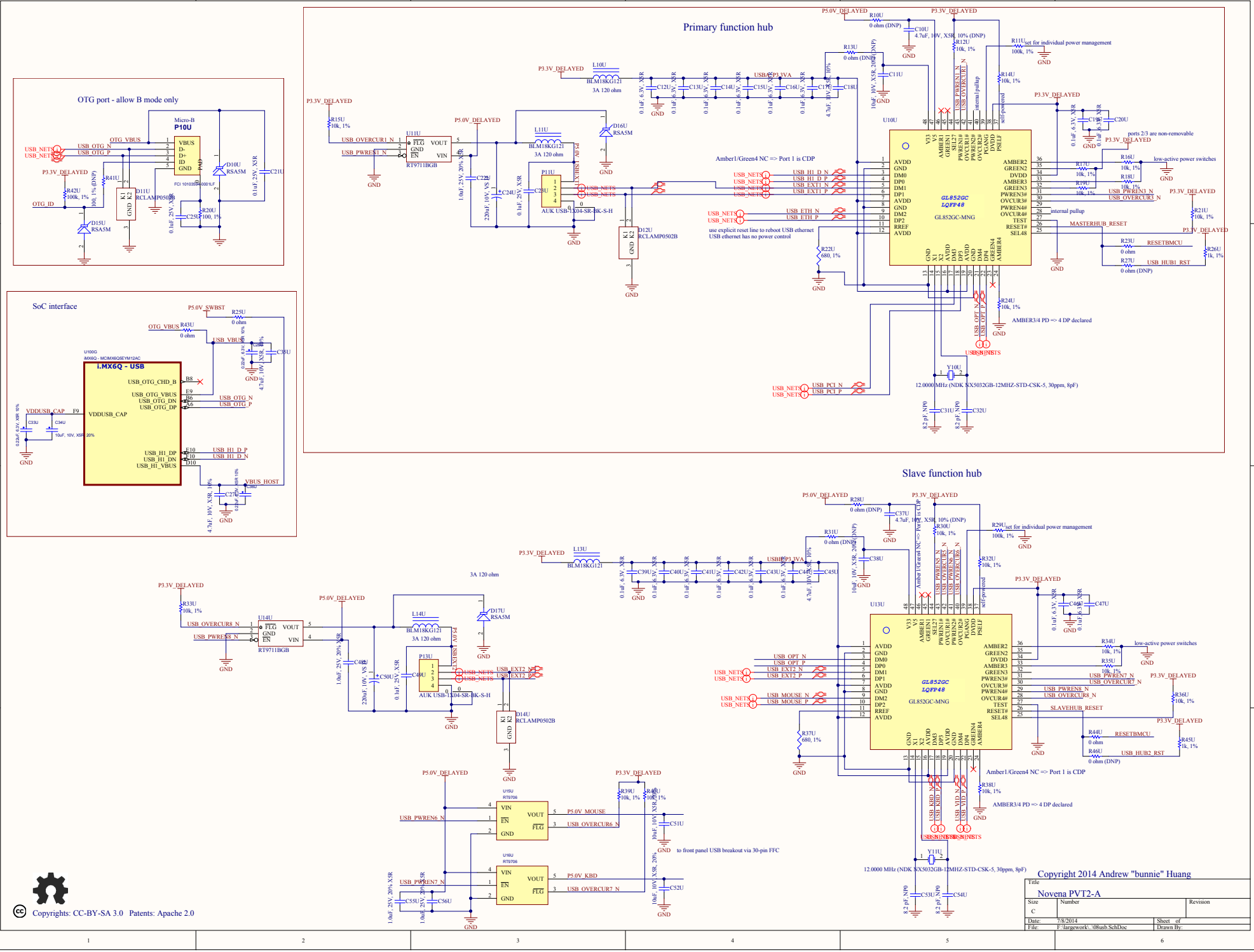
File: F:\largework\..\07sdcard.SchDoc		Drawn By:


OTG port - allow B mode only
Micro-B
P10U
OTG_VBUS
USB_OTG_N
USB_OTG_P
USB_NETS
USB_NETS
VBUS
D+
D+
ID
GND
PAD
FCI 10103594-0001LF
P3.3V_DELAYED
R41U
100, 1% (DNP)
R42U
100k, 1%
OTG_ID
D15U
RSA5M
K1
K2
GND
D11U
RCLAMP0502B
C25U
0.1uF, 25V, X5R
R20U
100, 1%
D10U
RSA5M
C21U
0.1uF, 25V, X5R
SoC interface
P5.0V_SWBST
R25U
0 ohm
OTG_VBUS
R43U
0 ohm
USB_VBUS
C35U
4.7uF, 10V, X5R, 10%
GND
U100G
IMX6Q - MCIMX6Q5EYM12AC
i.MX6Q - USB
USB_OTG_CHD_B
B8
USB_OTG_VBUS
E9
USB_OTG_DN
B6
USB_OTG_DP
A6
USB_OTG_N
USB_OTG_P
VDDUSB_CAP
F9
VDDUSB_CAP
C33U
0.22uF, 6.3V, X5R, 10%
C34U
10uF, 10V, X5R 20%
GND
USB_H1_DP
E10
USB_H1_DN
C10
USB_H1_VBUS
D10
USB_H1_D_P
USB_H1_D_N
VBUS_HOST
C26U
0.22uF
C27U
4.7uF, 10V, X5R, 10%
GND
Primary function hub
P5.0V_DELAYED
P3.3V_DELAYED
R10U
0 ohm (DNP)
C10U
4.7uF, 10V, X5R, 10% (DNP)
GND
R11U
set for individual power management
100k, 1%
GND
R13U
0 ohm (DNP)
C11U
10uF, 10V, X5R, 20% (DNP)
GND
P3.3V_DELAYED
L10U
BLM18KG121
3A 120 ohm
C12U
C13U
C14U
C15U
C16U
C17U
C18U
0.1uF, 6.3V, X5R
4.7uF, 10V, X5R, 10%
USB_P3.3VA
GND
U10U
USB_PWREN1_N
USB_OVERCUR1_N
internal pullup
self-powered
P3.3V_DELAYED
C19U
C20U
0.1uF, 6.3V, X5R
4.7uF, 6.3V, X5R
GND
ports 2/3 are non-removable
P3.3V_DELAYED
R14U
10k, 1%
P3.3V_DELAYED
R15U
10k, 1%
USB_OVERCUR1_N
USB_PWREN1_N
U11U
FLG
VOUT
GND
EN
VIN
RT9711BGB
GND
P5.0V_DELAYED
L11U
BLM18KG121
3A 120 ohm
D16U
RSA5M
GND
C22U
1.0uF, 25V, 20%, X5R
C24U
220uF, 10V, V5
C23U
0.1uF, 25V, X5R
P11U
AUK USB-1304-SR-BK-S-H
LXTHBST_A0.5d
USB_NETS
USB_NETS
K1
K2
GND
D12U
RCLAMP0502B
GND
Amber1/Green4 NC => Port 1 is CDP
USB_NETS
USB_NETS
USB_NETS
USB_NETS
USB_H1_D_N
USB_H1_D_P
USB_EXT1_N
USB_EXT1_P
USB_NETS
USB_NETS
USB_ETH_N
USB_ETH_P
use explicit reset line to reboot USB ethernet
USB ethernet has no power control
R22U
680, 1%
GND
AVDD
GND
DM0
DP0
DM1
DP1
AVDD
GND
DM2
DP2
RREF
AVDD
GL852GC
LQFP48
GL852GC-MNG
AMBER2
GREEN2
DVDD
AMBER3
GREEN3
PWREN3#
OVCUR3#
PWREN4#
OVCUR4#
TEST
RESET#
SEL48
R17U
10k, 1%
R19U
10k, 1%
R16U
10k, 1%
low-active power switches
R18U
10k, 1%
USB_PWREN3_N
USB_OVERCUR3_N
P3.3V_DELAYED
R21U
10k, 1%
internal pullup
MASTERHUB_RESET
P3.3V_DELAYED
R23U
0 ohm
RESETBMCU
R27U
0 ohm (DNP)
USB_HUB1_RST
R26U
1k, 1%
R24U
10k, 1%
AMBER3/4 PD => 4 DP declared
GND
USB_OPT_N
USB_OPT_P
USBSNKSNKS
Y10U
12.0000 MHz (NDK NX5032GB-12MHZ-STD-CSK-5, 30ppm, 8pF)
USB_NETS
USB_NETS
USB_PCI_N
USB_PCI_P
C31U
8.2 pF, NP0
C32U
8.2 pF, NP0
Slave function hub
P5.0V_DELAYED
P3.3V_DELAYED
R28U
0 ohm (DNP)
C37U
4.7uF, 10V, X5R, 10% (DNP)
GND
R29U
set for individual power management
100k, 1%
GND
R31U
0 ohm (DNP)
C38U
10uF, 10V, X5R, 20% (DNP)
GND
P3.3V_DELAYED
L13U
BLM18KG121
3A 120 ohm
C39U
C40U
C41U
C42U
C43U
C44U
C45U
0.1uF, 6.3V, X5R
4.7uF, 10V, X5R, 10%
USB_P3.3VA
GND
U13U
Amber1/Green4 NC => Port 1 is CDP
USB_PWREN5_N
USB_OVERCUR5_N
USB_PWREN7_N
USB_OVERCUR7_N
internal pullup
self-powered
P3.3V_DELAYED
C46U
C47U
0.1uF, 6.3V, X5R
4.7uF, 6.3V, X5R
GND
R32U
10k, 1%
P3.3V_DELAYED
R33U
10k, 1%
USB_OVERCUR8_N
USB_PWREN8_N
U14U
FLG
VOUT
GND
EN
VIN
RT9711BGB
GND
P5.0V_DELAYED
L14U
BLM18KG121
3A 120 ohm
D17U
RSA5M
GND
C48U
1.0uF, 25V, 20%, X5R
C50U
220uF, 10V, V5
C49U
0.1uF, 25V, X5R
P13U
AUK USB-1304-SR-BK-S-H
LXTHBST_A0.5d
USB_NETS
USB_NETS
USB_EXT2_N
USB_EXT2_P
GND
K1
K2
GND
D14U
RCLAMP0502B
GND
AVDD
GND
DM0
DP0
DM1
DP1
AVDD
GND
DM2
DP2
RREF
AVDD
GL852GC
LQFP48
GL852GC-MNG
AMBER2
GREEN2
DVDD
AMBER3
GREEN3
PWREN3#
OVCUR3#
PWREN4#
OVCUR4#
TEST
RESET#
SEL48
R34U
10k, 1%
low-active power switches
R35U
10k, 1%
USB_PWREN7_N
USB_OVERCUR7_N
P3.3V_DELAYED
R36U
10k, 1%
USB_PWREN8_N
USB_OVERCUR8_N
SLAVEHUB_RESET
P3.3V_DELAYED
R44U
0 ohm
RESETBMCU
R46U
0 ohm (DNP)
USB_HUB2_RST
R45U
1k, 1%
R37U
680, 1%
GND
USB_NETS
USB_NETS
USB_MOUSE_N
USB_MOUSE_P
USB_NETS
USB_NETS
USB_EXT2_N
USB_EXT2_P
Amber1/Green4 NC => Port 1 is CDP
R38U
10k, 1%
AMBER3/4 PD => 4 DP declared
GND
USB_KBD_N
USB_KBD_P
USB_VID_N
USB_VID_P
USBSNKSNKSNKSNKS
Y11U
12.0000 MHz (NDK NX5032GB-12MHZ-STD-CSK-5, 30ppm, 8pF)
C53U
8.2 pF, NP0
C54U
8.2 pF, NP0
P5.0V_DELAYED
P3.3V_DELAYED
U15U
RT9706
VIN
EN
GND
VOUT
FLG
USB_PWREN6_N
P5.0V_MOUSE
USB_OVERCUR6_N
R39U
10k, 1%
R40U
10k, 1%
C51U
10uF, 10V
GND
to front panel USB breakout via 30-pin FFC
U16U
RT9706
USB_PWREN7_N
P5.0V_KBD
USB_OVERCUR7_N
C55U
1.0uF, 25V, 20%, X5R
C56U
10uF, 10V, X5R, 20%
C52U
10uF, 10V, X5R, 20%
GND
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Title
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Number
Revision
Date:
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F:\largework\..\08usb.SchDoc
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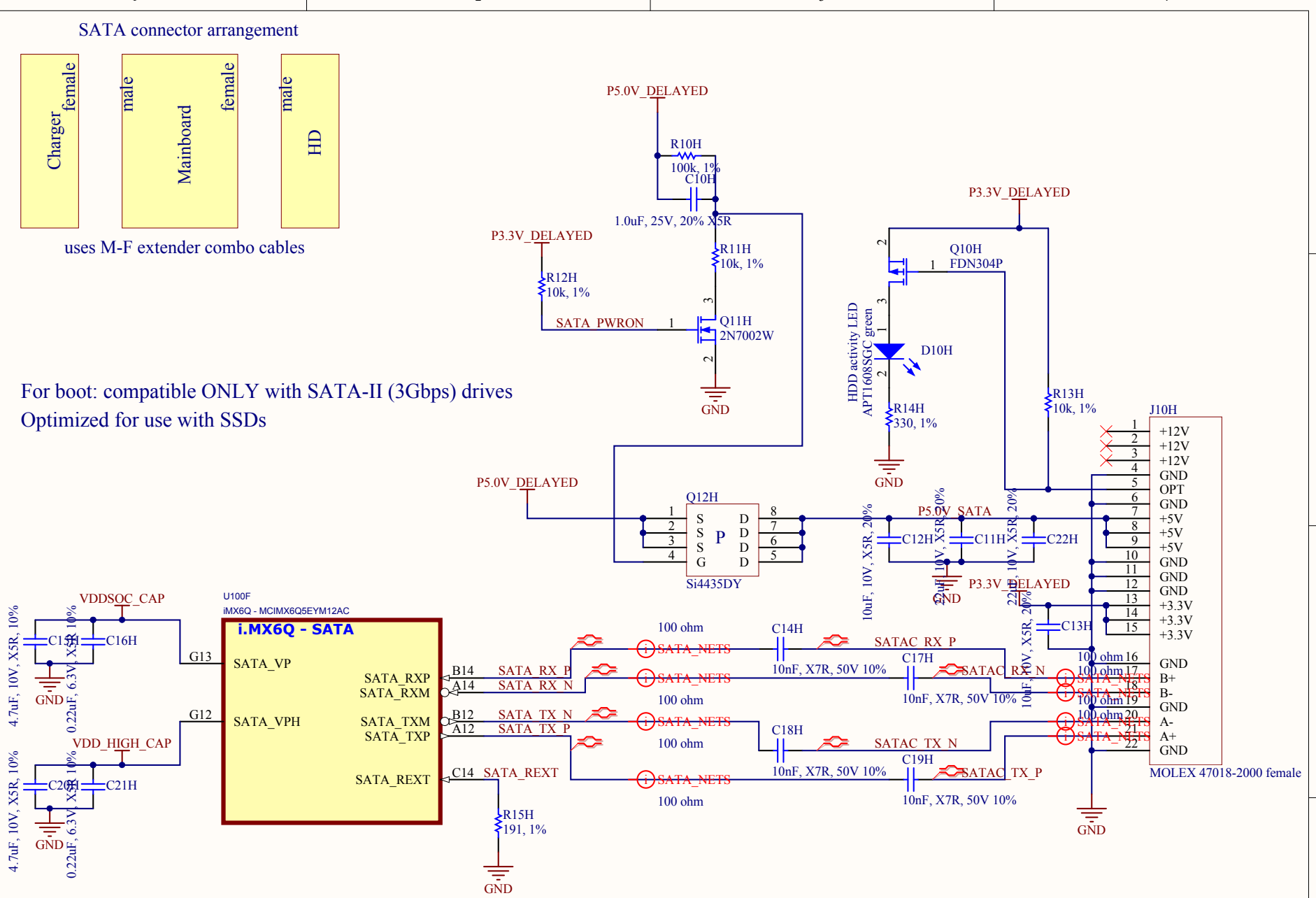
SATA connector arrangement
Charger
female
male
Mainboard
female
male
HD
uses M-F extender combo cables
For boot: compatible ONLY with SATA-II (3Gbps) drives
Optimized for use with SSDs
P5.0V_DELAYED
R10H
100k, 1%
C10H
1.0uF, 25V, 20% X5R
P3.3V_DELAYED
R11H
10k, 1%
R12H
10k, 1%
SATA_PWRON
Q11H
2N7002W
GND
P3.3V_DELAYED
Q10H
FDN304P
HDD activity LED
APT1608SGC green
D10H
R14H
330, 1%
GND
R13H
10k, 1%
P5.0V_DELAYED
Q12H
Si4435DY
P5.0V_SATA
C12H
C11H
C22H
10uF, 10V, X5R, 20%
10V, X5R, 20%
22uF, 10V, X5R, 20%
GND
P3.3V_DELAYED
C13H
J10H
+12V
+12V
+12V
GND
OPT
GND
+5V
+5V
+5V
GND
GND
GND
+3.3V
+3.3V
+3.3V
GND
B+
B-
GND
A-
A+
GND
MOLEX 47018-2000 female
VDDSOC_CAP
C15H
C16H
4.7uF, 10V, X5R, 10%
0.22uF, 6.3V, X5R, 10%
GND
VDD_HIGH_CAP
C20H
C21H
4.7uF, 10V, X5R, 10%
0.22uF, 6.3V, X5R, 10%
GND
U100F
iMX6Q - MCIMX6Q5EYM12AC
i.MX6Q - SATA
G13
G12
SATA_VP
SATA_VPH
SATA_RXP
SATA_RXM
SATA_TXM
SATA_TXP
SATA_REXT
B14
SATA_RX_P
A14
SATA_RX_N
B12
SATA_TX_N
A12
SATA_TX_P
C14
SATA_REXT
R15H
191, 1%
GND
100 ohm
SATA_NETS
C14H
10nF, X7R, 50V 10%
SATAC_RX_P
C17H
SATAC_RX_N
C18H
SATAC_TX_N
C19H
SATAC_TX_P
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Size
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Number
Revision
Date: 7/8/2014
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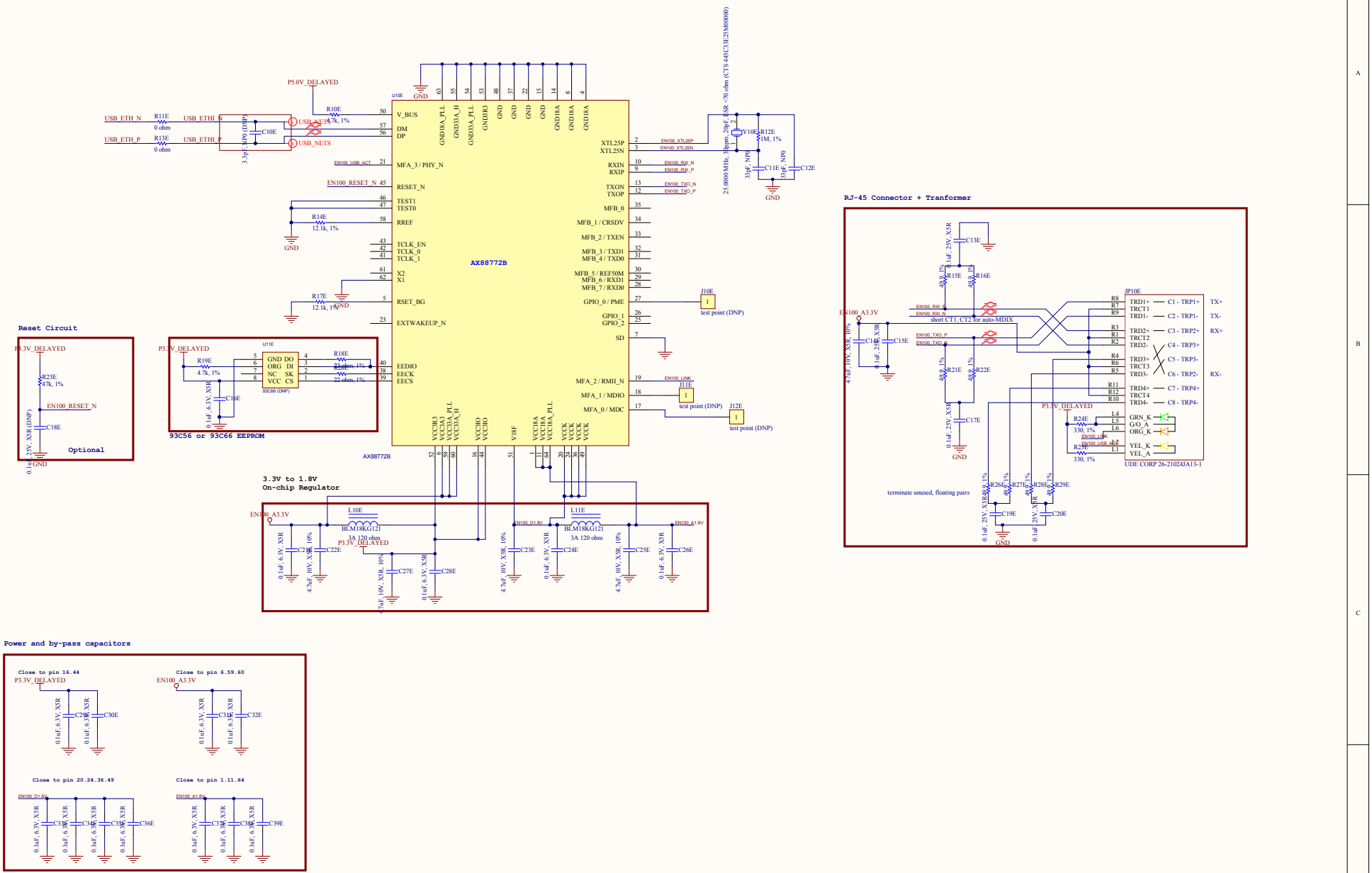

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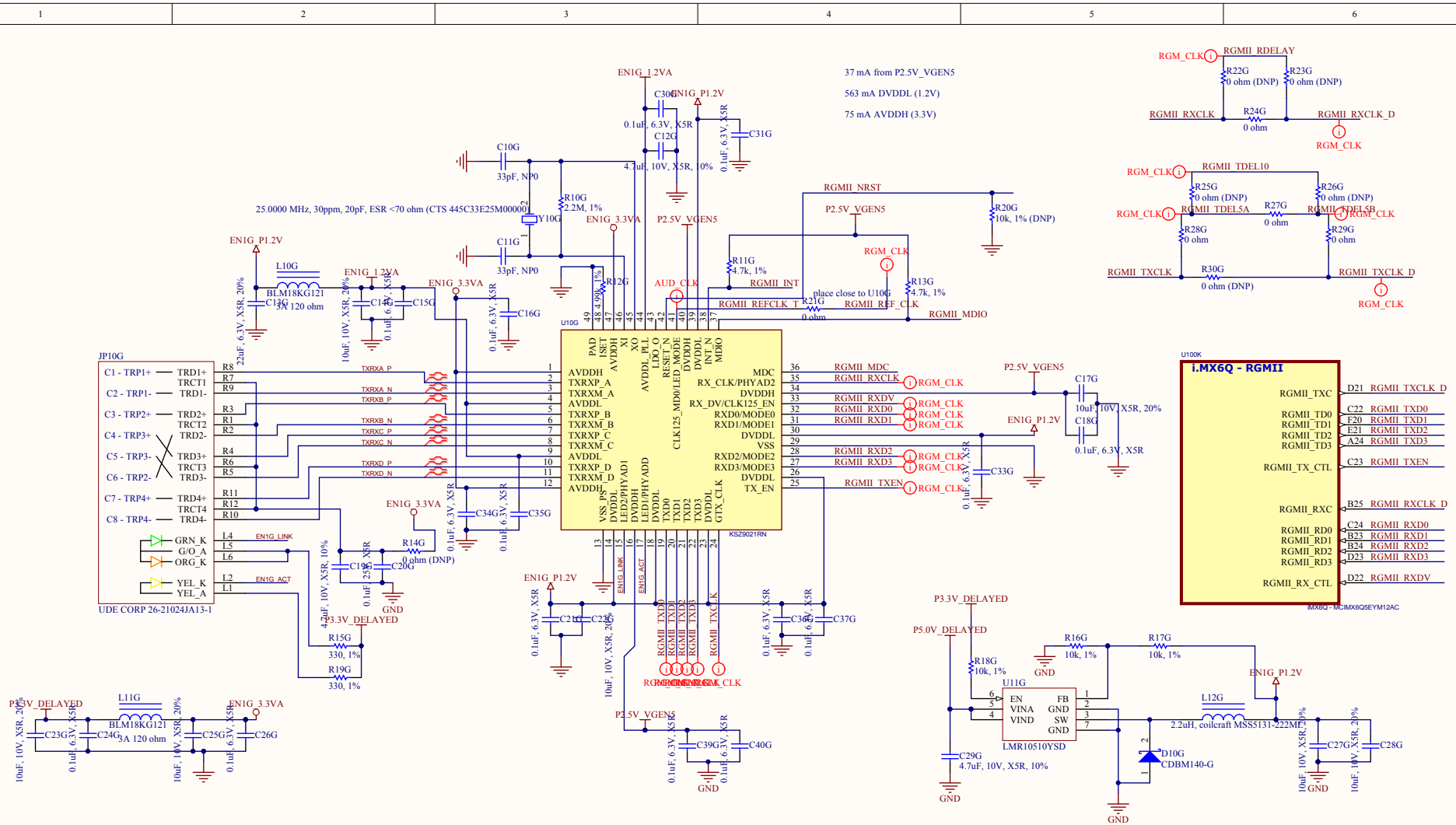
37 mA from P2.5V_VGEN5
563 mA DVDDL (1.2V)
75 mA AVDDH (3.3V)
25.0000 MHz, 30ppm, 20pF, ESR <70 ohm (CTS 445C33E25M00000)
KSZ9021RN
U10G
JP10G
UDE CORP 26-21024JA13-1
U100K
i.MX6Q - RGMII
IMX6Q - MCIMX6QSEYM12AC
U11G
LMR10510YSD
place close to U10G
2.2uH, coilcraft MSS5131-222ME
CDBM140-G
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Novena PVT2-A
Size B
Number
Revision
Date: 7/8/2014
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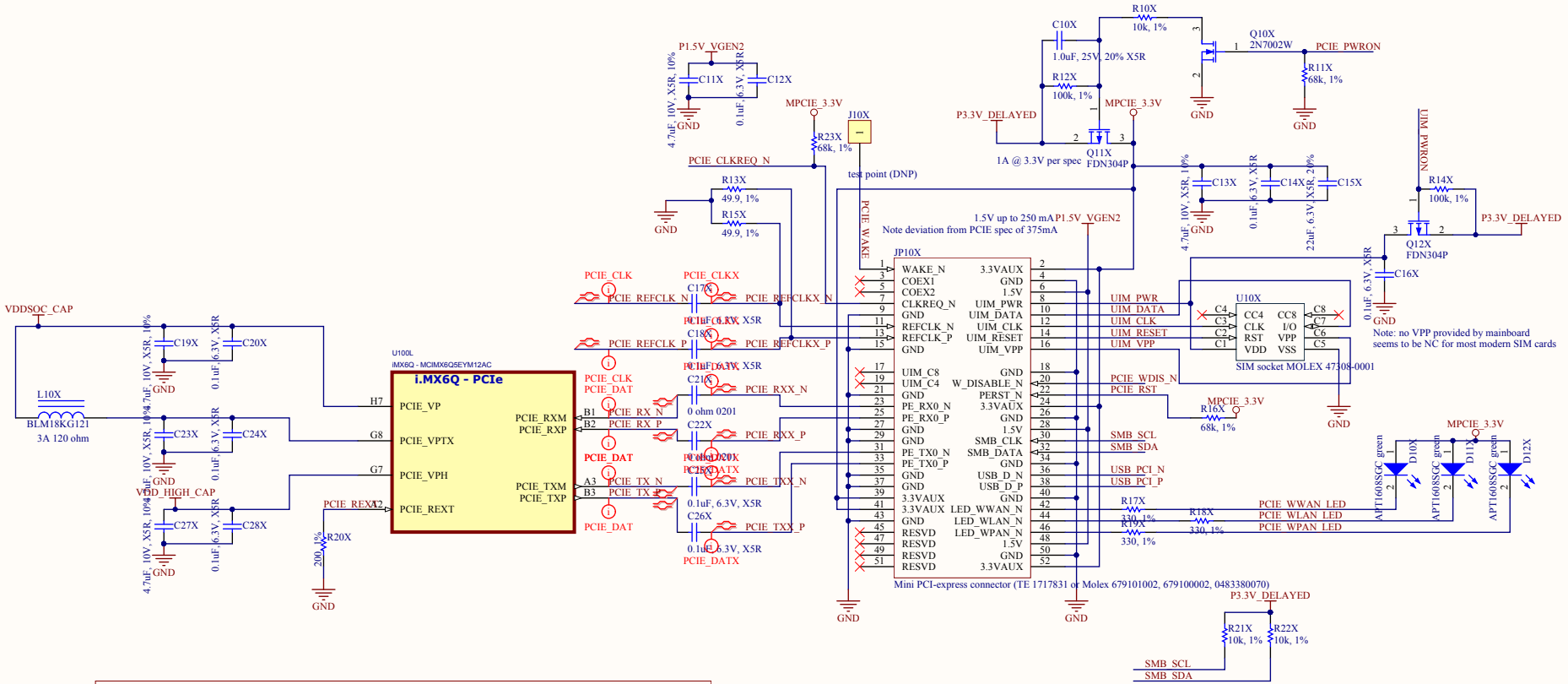

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Title: Novena PVT2-A		
Size: B	Number	Revision
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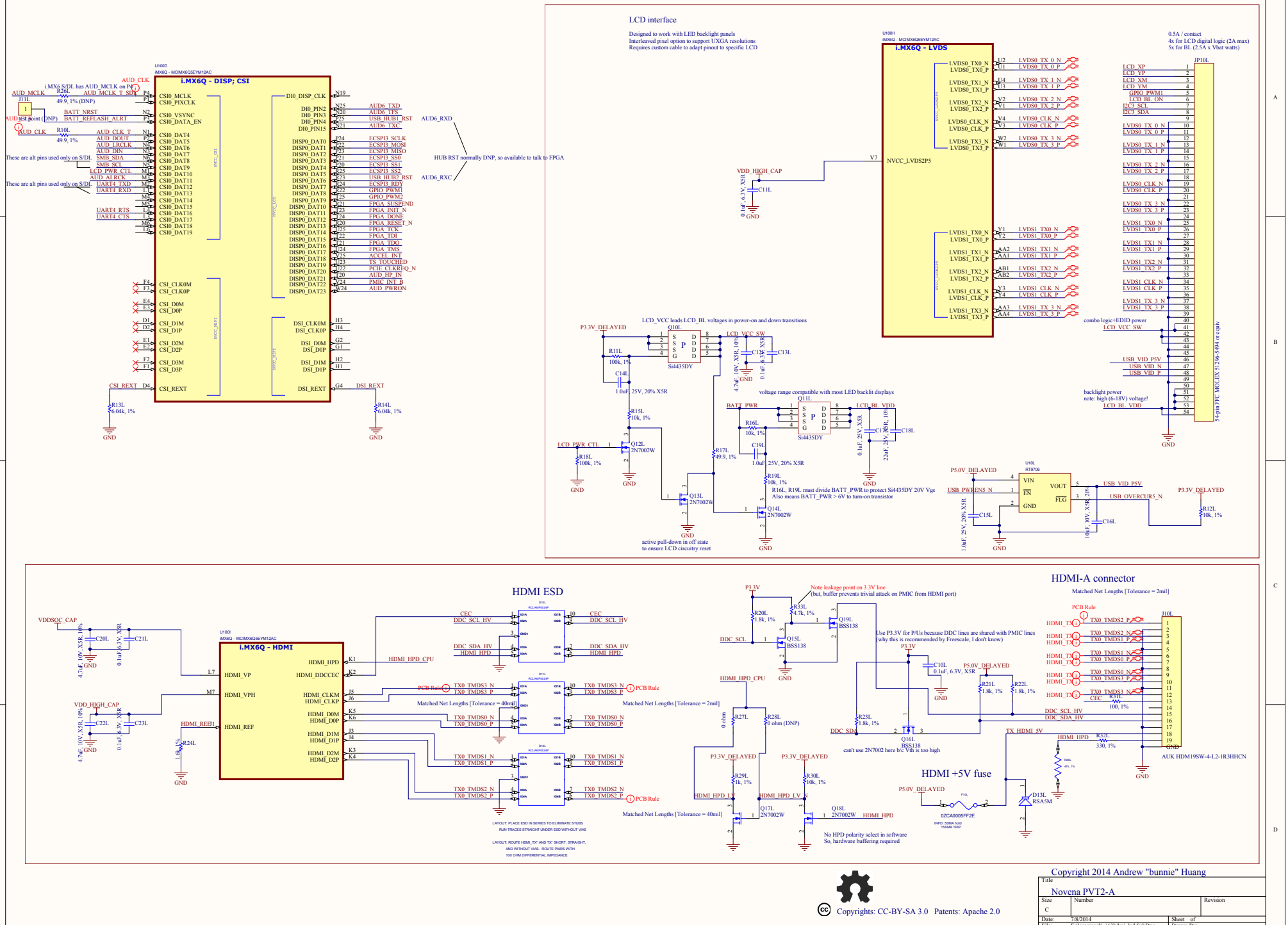
File: F:\largework\..\12mPCIe.SchDoc		Drawn By:


LCD interface
Designed to work with LED backlight panels
Interleaved pixel option to support UXGA resolutions
Requires custom cable to adapt pinout to specific LCD
i.MX6Q - DISP; CSI
i.MX6Q - LVDS
i.MX6Q - HDMI
HDMI ESD
HDMI-A connector
HDMI +5V fuse
LCD_VCC leads LCD_BL voltages in power-on and down transitions
voltage range compatible with most LED backlit displays
R16L, R19L must divide BATT_PWR to protect Si4435DY 20V Vgs
Also means BATT_PWR > 6V to turn-on transistor
active pull-down in off state
to ensure LCD circuitry reset
0.5A / contact
4x for LCD digital logic (2A max)
5x for BL (2.5A x Vbat watts)
54-pin FFC MOLEX 51296-5094 or equiv
combo logic+EDID power
backlight power
note: high (6-18V) voltage!
Note leakage point on 3.3V line
(but, buffer prevents trivial attack on PMIC from HDMI port)
Use P3.3V for P/Us because DDC lines are shared with PMIC lines
(why this is recommended by Freescale, I don't know)
can't use 2N7002 here b/c Vth is too high
No HPD polarity select in software
So, hardware buffering required
Matched Net Lengths [Tolerance = 40mil]
Matched Net Lengths [Tolerance = 2mil]
AUK HDM19SW-4-L2-1R3HHCN
0ZCA0005FF2E
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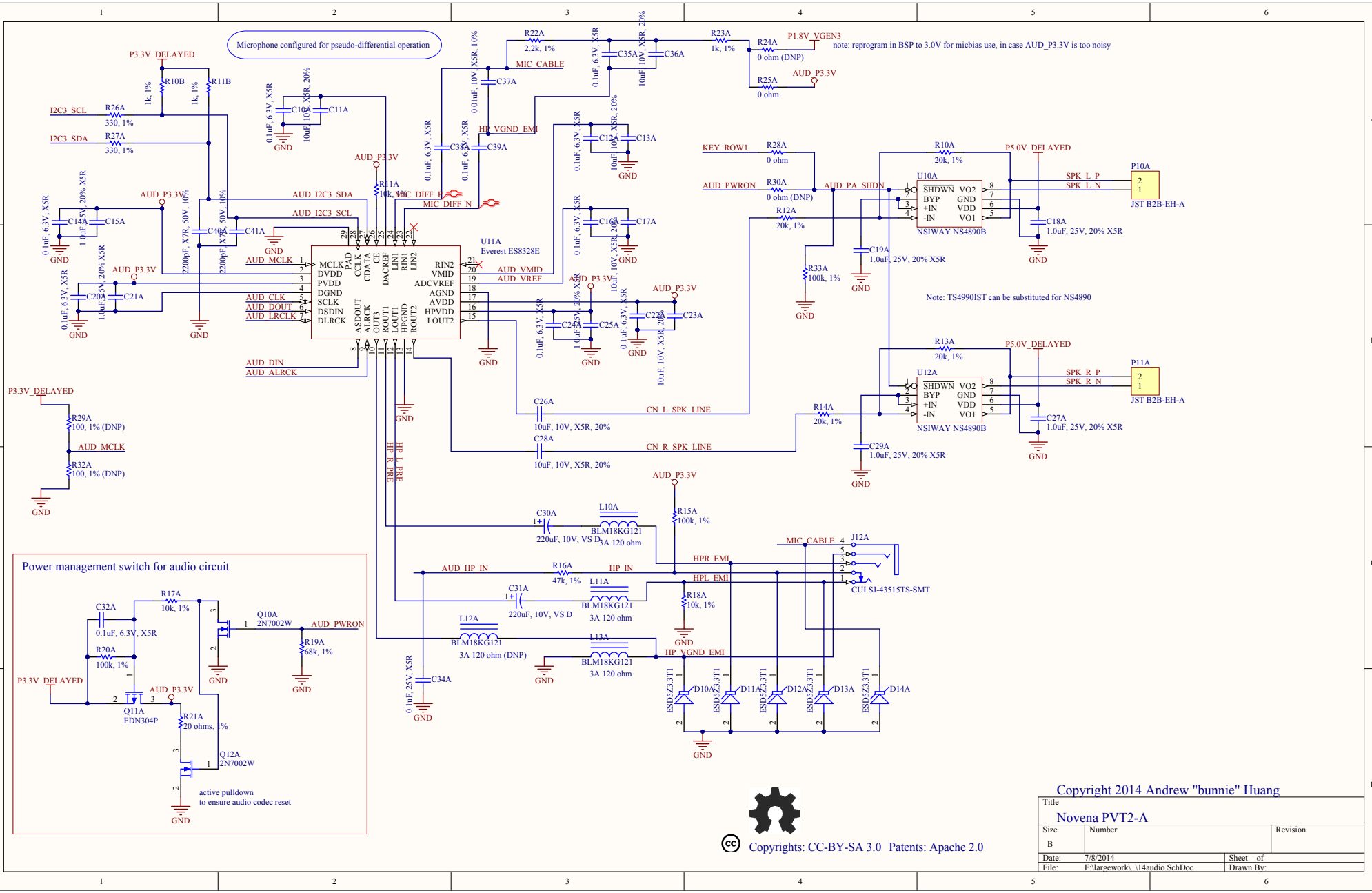
Novena PVT2-A
7/8/2014
F:\largework\..\13hdmi_lcd.SchDoc


Microphone configured for pseudo-differential operation
P3.3V_DELAYED
R10B
R11B
1k, 1%
I2C3_SCL
I2C3_SDA
R26A
R27A
330, 1%
R22A
2.2k, 1%
MIC_CABLE
C37A
HP_VGND_EMI
C35A
C36A
0.1uF, 6.3V, X5R
10uF 10V, X5R, 20%
R23A
R24A
0 ohm (DNP)
R25A
0 ohm
P1.8V_VGEN3
note: reprogram in BSP to 3.0V for micbias use, in case AUD_P3.3V is too noisy
AUD_P3.3V
C10A
C11A
C38A
C39A
C12A
C13A
C14A
C15A
C40A
C41A
R11A
10k, 1%
MIC_DIFF_P
MIC_DIFF_N
C16A
C17A
AUD_I2C3_SDA
AUD_I2C3_SCL
U11A
Everest ES8328E
AUD_MCLK
AUD_DOUT
AUD_LRCLK
AUD_CLK
AUD_DIN
AUD_ALRCK
AUD_VMID
AUD_VREF
C20A
C21A
C24A
C25A
C23A
KEY_ROW1
R28A
AUD_PWRON
R30A
AUD_PA_SHDN
R12A
20k, 1%
R10A
P5.0V_DELAYED
U10A
NSIWAY NS4890B
SPK_L_P
SPK_L_N
P10A
JST B2B-EH-A
C18A
1.0uF, 25V, 20% X5R
C19A
R33A
100k, 1%
Note: TS4990IST can be substituted for NS4890
R13A
U12A
SPK_R_P
SPK_R_N
P11A
C27A
C29A
R14A
C26A
CN_L_SPK_LINE
C28A
CN_R_SPK_LINE
HP_L_PRE
HP_R_PRE
R29A
100, 1% (DNP)
R32A
C30A
220uF, 10V, VS D
L10A
BLM18KG121
3A 120 ohm
R15A
100k, 1%
MIC_CABLE
J12A
CUI SJ-43515TS-SMT
HPR_EMI
HPL_EMI
AUD_HP_IN
R16A
47k, 1%
HP_IN
C31A
L11A
R18A
10k, 1%
L12A
BLM18KG121
3A 120 ohm (DNP)
L13A
C34A
D10A
D11A
D12A
D13A
D14A
ESD5Z3.3T1
Power management switch for audio circuit
R17A
10k, 1%
C32A
0.1uF, 6.3V, X5R
Q10A
2N7002W
R19A
68k, 1%
R20A
100k, 1%
Q11A
FDN304P
R21A
20 ohms, 1%
Q12A
2N7002W
active pulldown
to ensure audio codec reset
GND
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Title
Novena PVT2-A
Size
B
Number
Revision
Date: 7/8/2014
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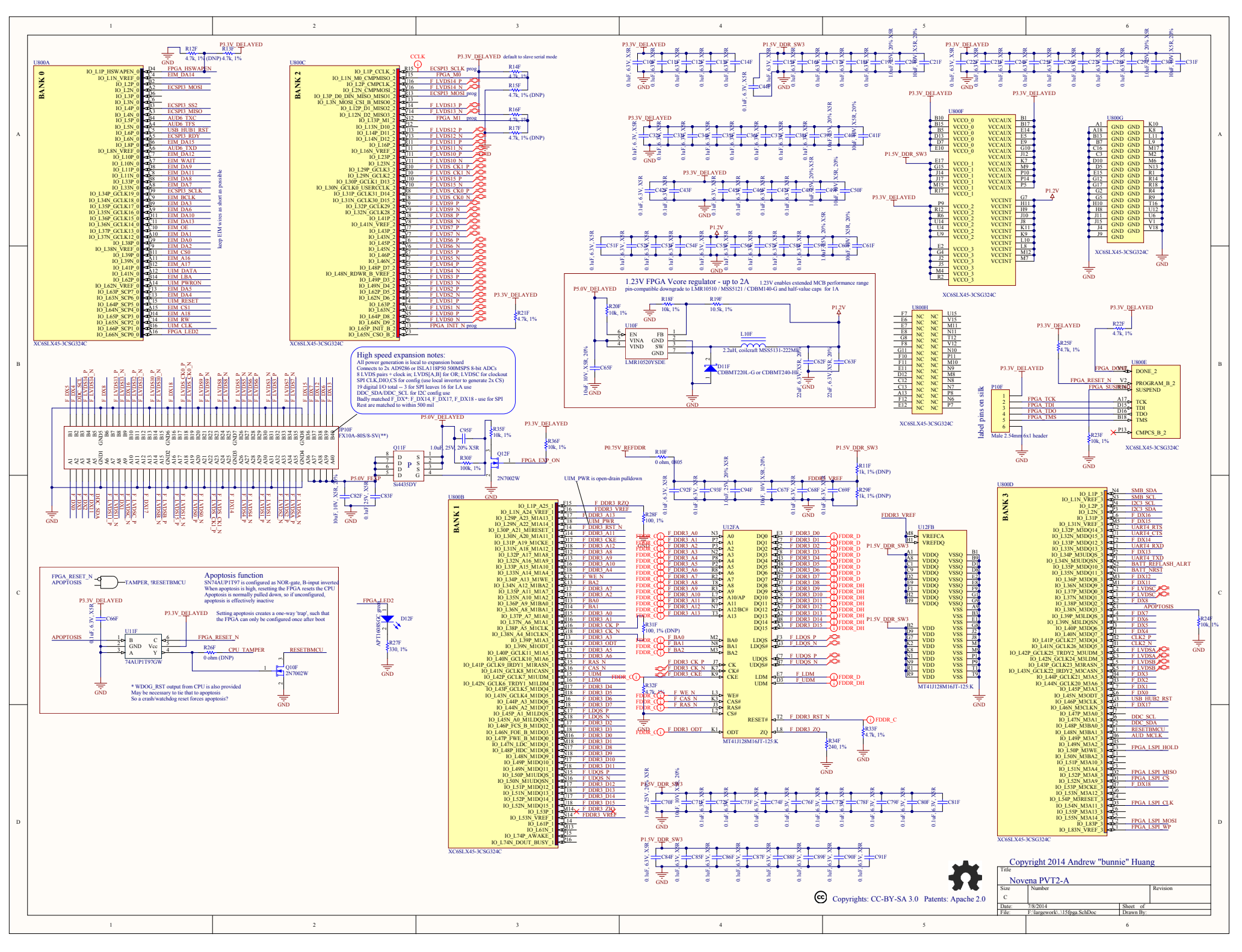
BANK 0
BANK 2
BANK 1
BANK 3
XC6SLX45-3CSG324C
High speed expansion notes:
All power generation is local to expansion board
Connects to 2x AD9286 or ISLA118P50 500MSPS 8-bit ADCs
8 LVDS pairs + clock in; LVDS[A,B] for OR; LVDSC for clockout
SPI CLK,DIO,CS for config (use local inverter to generate 2x CS)
19 digital I/O total -- 3 for SPI leaves 16 for LA use
DDC_SDA/DDC_SCL for I2C config use
Badly matched F_DX*- F_DX14, F_DX17, F_DX18 - use for SPI
Rest are matched to within 500 mil
1.23V FPGA Vcore regulator - up to 2A
1.23V enables extended MCB performance range
pin-compatible downgrade to LMR10510 / MSS5121 / CDBM140-G and half-value caps for 1A
LMR10520YSDE
2.2uH, coilcraft MSS5131-222ME
CDBMT2220L-G or CDBMT240-HF
Apoptosis function
SN74AUP1T97 is configured as NOR-gate, B-input inverted
When apoptosis is high, resetting the FPGA resets the CPU
Apoptosis is normally pulled down, so if unconfigured, apoptosis is effectively inactive
Setting apoptosis creates a one-way 'trap', such that the FPGA can only be configured once after boot
* WDOG_RST output from CPU is also provided
May be necessary to tie that to apoptosis
So a crash/watchdog reset forces apoptosis?
label pins on silk
Male 2.54mm 6x1 header
UIM_PWR is open-drain pulldown
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Revision
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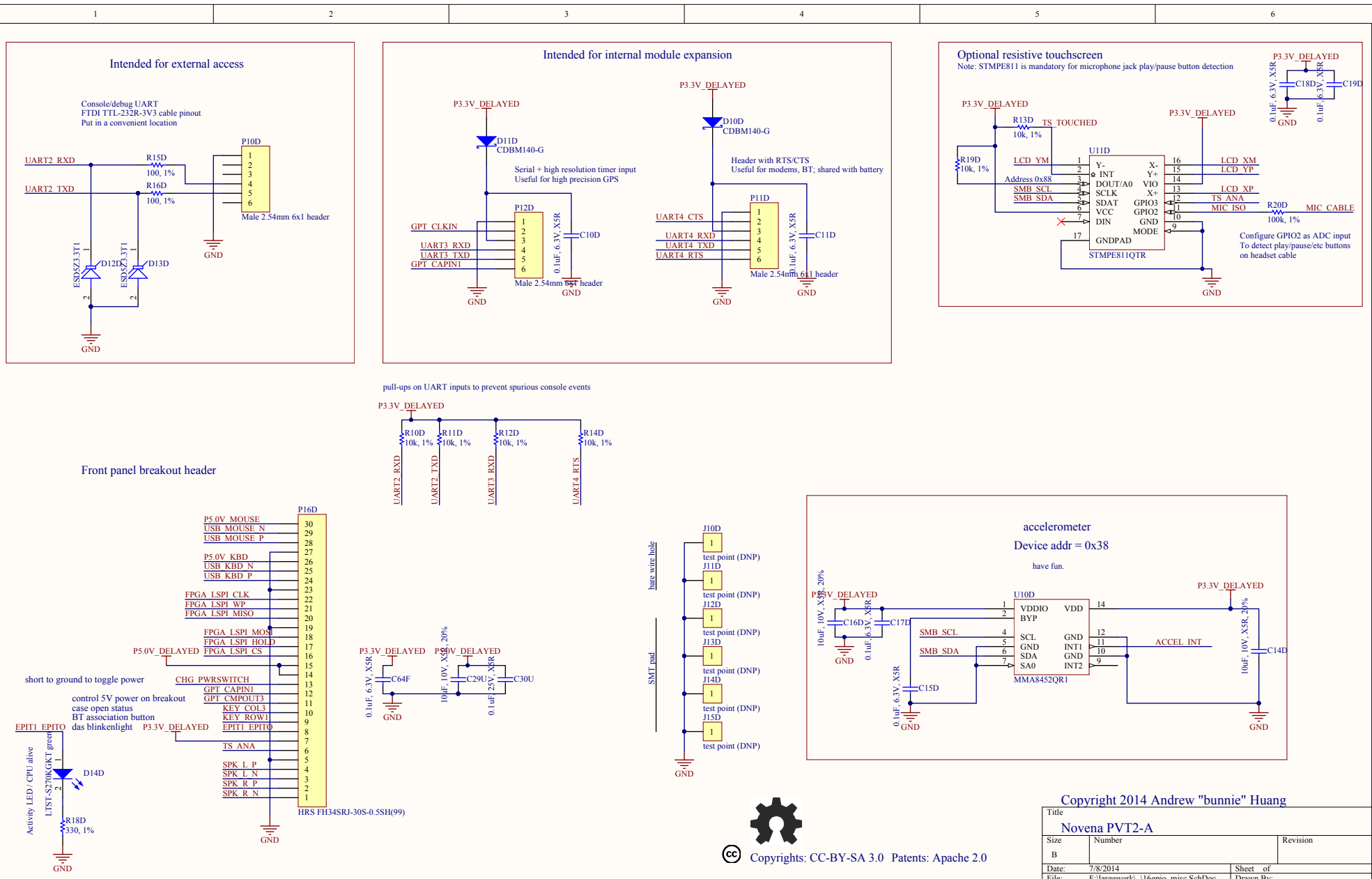
Intended for external access
Console/debug UART
FTDI TTL-232R-3V3 cable pinout
Put in a convenient location
UART2_RXD
UART2_TXD
R15D
100, 1%
R16D
100, 1%
P10D
Male 2.54mm 6x1 header
ESD5Z3.3T1
D12D
D13D
GND
Intended for internal module expansion
P3.3V_DELAYED
D11D
CDBM140-G
Serial + high resolution timer input
Useful for high precision GPS
P12D
GPT_CLKIN
UART3_RXD
UART3_TXD
GPT_CAPIN1
C10D
0.1uF, 6.3V, X5R
Male 2.54mm 6x1 header
D10D
CDBM140-G
Header with RTS/CTS
Useful for modems, BT; shared with battery
P11D
UART4_CTS
UART4_RXD
UART4_TXD
UART4_RTS
C11D
Male 2.54mm 6x1 header
Optional resistive touchscreen
Note: STMPE811 is mandatory for microphone jack play/pause button detection
C18D
C19D
R13D
10k, 1%
TS_TOUCHED
R19D
10k, 1%
LCD_YM
Address 0x88
SMB_SCL
SMB_SDA
U11D
Y-
INT
DOUT/A0
SCLK
SDAT
VCC
DIN
X-
Y+
VIO
X+
GPIO3
GPIO2
GND
MODE
GNDPAD
STMPE811QTR
LCD_XM
LCD_YP
LCD_XP
TS_ANA
MIC_ISO
R20D
100k, 1%
MIC_CABLE
Configure GPIO2 as ADC input
To detect play/pause/etc buttons
on headset cable
pull-ups on UART inputs to prevent spurious console events
R10D
10k, 1%
R11D
10k, 1%
R12D
10k, 1%
R14D
10k, 1%
UART2_RXD
UART2_TXD
UART3_RXD
UART4_RTS
Front panel breakout header
P16D
P5.0V_MOUSE
USB_MOUSE_N
USB_MOUSE_P
P5.0V_KBD
USB_KBD_N
USB_KBD_P
FPGA_LSPI_CLK
FPGA_LSPI_WP
FPGA_LSPI_MISO
FPGA_LSPI_MOSI
FPGA_LSPI_HOLD
FPGA_LSPI_CS
P5.0V_DELAYED
short to ground to toggle power
CHG_PWRSWITCH
control 5V power on breakout
case open status
BT association button
das blinkenlight
GPT_CAPIN1
GPT_CMPOUT3
KEY_COL3
KEY_ROW1
EPIT1_EPITO
P3.3V_DELAYED
TS_ANA
SPK_L_P
SPK_L_N
SPK_R_P
SPK_R_N
HRS FH34SRJ-30S-0.5SH(99)
EPIT1_EPITO
Activity LED / CPU alive
LTST-S270KGKT green
D14D
R18D
330, 1%
C64F
C29U
C30U
0.1uF, 6.3V, X5R
10uF, 10V, X5R, 20%
0.1uF, 25V, X5R
J10D
J11D
J12D
J13D
J14D
J15D
test point (DNP)
bare wire hole
SMT pad
accelerometer
Device addr = 0x38
have fun.
C16D
C17D
C15D
U10D
VDDIO
BYP
SCL
GND
SDA
SA0
VDD
GND
INT1
GND
INT2
MMA8452QR1
SMB_SCL
SMB_SDA
ACCEL_INT
C14D
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Title
Novena PVT2-A
Size
B
Number
Revision
Date: 7/8/2014
Sheet of
File: F:\largework\..\16gpio_misc.SchDoc
Drawn By: