Novena PVT2 ECO List

From Studio Kousagi Wiki

This is a list of all the changes applied to the board from PVT1 to PVT2 (Crowd Supply initial campaign) release. If it's not on this list, it didn't happen.

Each change has the format of issue summary/resolution, and specific change

Contents

ECO1: Improve HPD margin

HPD on i.MX6 has a low impedance (10k). This causes marginal HPD performance on some boards. Make R29L stronger.

PVT1	PVT2	Notes
R29L 10k, 1% / REC1005N	R29L 1k, 1%	HDMI HPD perforance

ECO2: EOL issue U11D

STMPE610 is EOL. Switch to STMPE811, pin-compatible and not EOL.

PVT1	PVT2	Notes
U11D STMPE610	U11D STMPE811QTR	resolve EOL issue

ECO3: EOL issue audio amplifier

NS4890 is EOL. Replace with compatible NS4890B in two places.

PVT1	PVT2	Notes
U10A, U12A NS4890	U10A, U12A NS4890B	resolve EOL issue

ECO4: Improve kernel panic logging

U10S is too small for good kernel panic logging. Replace with larger capacity I2C EEPROM to store several crashes worth of logs.

PVT1	PVT2	Notes
U10S 24LC32A-I/ST	U10S FT24C512AUTR-T	improve KP logging

ECO5: 47uF 1206 capacitor is wrong AGAIN

The wrong package type (1210) is being ordered for this 1206 part. This was supposed to be corrected on PVT1. Please double-confirm that instruction is understood that this part cannot be substituted with a 1210 footprint.

DVT and PVT1	PVT2	Notes
C43M 47uF, 6.3V, 20% X5R	47uF, 6.3V, 20% X5R (CL31A476MQHNNNE)	double-confirm this change is understood!
C44M 47uF, 6.3V, 20% X5R	47uF, 6.3V, 20% X5R (CL31A476MQHNNNE)	
C45M 47uF, 6.3V, 20% X5R	47uF, 6.3V, 20% X5R (CL31A476MQHNNNE)	
C18M 47uF, 6.3V, 20% X5R	47uF, 6.3V, 20% X5R (CL31A476MQHNNNE)	
C52C 47uF, 6.3V, 20% X5R	47uF, 6.3V, 20% X5R (CL31A476MQHNNNE)	

ECO6: Upgrade accelerometer

Old accelerometer is probably approaching EOL.

MMA8452Q is stocked at 3mm+ levels in the factory and has existing Linux drivers in main-line. A little more expensive than MMA8653FC, but twenty cents is not going to kill this product. So, we go with MMA8452Q.

PVT1	PVT2	Notes
U10D MMA7455L	U10D MMA8452Q	improve accelerometer, avoid EOL
R17D 20k, 1%	removed	INT output is now push/pull

ECO7: Upgrade FAN53540UCX

FAN53540UCX marked as not recommended for new designs.

FAN53541UCX is a pin-compatible upgrade. Difference between the two is that the enable and mode input no longer need 1k ballast resistors. However, leaving them in place causes no harm and allows for downgrade compatibility in case parts are in short supply.

PVT1	PVT2	Notes
U13N FAN533540UCX	U13N FAN53541UCX	

ECO8: Update i.MX6 P/N

Previously schematic listed the 1.0GHz P/N as the default. Updated to reflect the plan to only produce with the 1.2GHz P/N.

PVT1	PVT2	Notes
U100 iMX6Q - PCIMX6Q5EVT10AD	U100 iMX6Q - MCIMX6Q5EYM12AC	

ECO9: Confirm change of D10C

Measurements on diode leakage indicate D10C was not properly updated on BOM at last ECO. Confirm factory received ECO update.

DVT/PVT1	PVT2	Notes
D10C NSR0320	D10C RB751V40,115	Reduce leakage from 1mA max to 0.0005mA max; peak If = 120mA, but max current on stby line is ~1mA

ECO10: U12N is EOL

U12N, the lower synchronous switch of the 5V converter, has gone EOL. Replace with recommended substitute by On Semi.

The recommended substitute NTMFS4C35NT1G is pin-compatible. It has a slightly lower power rating due to a higher Tj to the case, but the RdsON is the same. The converter is actually highly over-spec'd for the measured loads, so this substitution is not a problem. In fact, the substitute may improve efficiency slightly as the gate charge and other parasitics of the new device are lower.

PVT1	PVT2	Notes
U12N NTMFS4935NT1G	U12N NTMFS4C35NT1G	

ECO11: Remove AW-NU137 option

AW-NU137 is EOL and also, we're just never going to use it. It was originally included as an option for wifi in devices that needed to be cheap and where it was acceptable to not have PCIe and also binary blobs are acceptable. There has been zero demand for this configuration option.

Also, swap USB_PCI with USB_VID ports on upstream hub for improved routability. This should have no impact on the software.

PVT1	PVT2	Notes
P12U 2mm 5-pin male header	remove	
D13U RSA5M	remove	
U12U RT9706	remove	
C26U 1.0uF, 25V, 20% X5R	remove	
R23U 10k, 1%	remove	
R26U 0 ohm	remove	replace with permanent traces
R27U 0 ohm	remove	replace with permanent traces

ECO12: Fix CDP issue on USB port EXT2

USB port EXT2 has 1.5A-capable limits but does not configure itself as CDP. Fix this by swapping Port4 (EXT2 on PVT1) for Port 1 (USB_VID on PVT1). Amber1/Green4 NC (as currently configured) sets only Downstream Port 1 as CDP-capable.

This is purely a wire fix, no BOM-visible ECO required.

ECO13: Improve inductor profile

The ferrite MSS1260 used as the primary power inductor is a bit too tall and large. Use a composite molded core XAL7030 which is a bit more compact.

Pros/cons: XAL7030 has a better rated Irms than MSS1260, but seems mostly due to better heat conduction out of the package, not due to better electrical performance. The DCR of XAL7030 is 19.5mOhm, MSS1260 is 12.60mOhm, so conduction losses are greater. Isat of the XAL7030 is better due to soft-saturating characteristic of the composite core. Overall, I expect there to be very little change in practical circuit performance, perhaps a 1-2% max loss in battery life with this change under Ipeak conditions.

The MSS1260 isn't removed from the PCB layout. Instead, XAL7030 shall be fitted inside the footprint of the MSS1260. This allows for going back to the original inductor in case there is a design issue with the XAL7030.

This change is coordinated onto Senoko BOM as well.

PVT1	PVT2	Notes
L10N 3.3uH, MSS1260-332NL	L10N 3.3uH, MSS1260-332NL (DNP)	remove from BOM but leave footprint
add	L10NB 3.3uH, XAL7030-332MEC	add inductor within old footprint

ECO14: Rework front panel connector

For integration with laptop, a unified front panel connector is introduced.

P16D (8-pin FH19SC from Hirose) is removed. All signals from this connector are re-routed to a new P16D, now an HRS FH34SRJ-30S-0.5SH.

This 30-pin header now contains the following features:

- both USB ports going to the front panel
- 6x GPIO routed from the FPGA (so as to emulate at least SPI (with WP/HOLD), 3x I2C, or just function as 6x GPIO)
- TS_ANA analog input
- power routing for prototyping convenience
- some CPU GPIO to provide for blinkenlight on the front panel
- the power switch from Senoko (to turn the system on and off from the front panel)
- a front panel general purpose switch (to allow for recovery boot and BT keyboard association)
- speakers (original headers still retained) to allow for cleaner in-case routing of wires

The major downside of this revision is the internal USB headers can no longer be tapped using a simple DIY 8-pin ribbon cable. However, the 8-pin ribbon cable was found to have inadequate performance for stable USB2.0 operation anyways.

U14F was sacrificed. It's a SPI ROM that hangs off the FPGA, which has never been used in any design. The intention of U14F was to store private keys or other local NV storage for the FPGA that was off hard-drive. Instead, the SPI pins are run to the 30-pin header so users can have more flexibility on what SPI device to attach (you can still attach a device similar to U14F, but now it can be anything else as well).

PVT1	PVT2	Notes
P16D HRS FH19SC-8S-0.5SH(05)	P16D HRS FH34SRJ-30S-0.5SH(99)	upgrade header to more pins
P14U Male right angle 4x2 2.54mm header	removed	replaced with 30-pin header
U14F MX25L512EMI-10G	removed	route signals to 30-pin header instead
P_LSPI_WP	removed	
added	R39N 330, 1%	ballast on CHG_PWRSWITCH
C75F 0.1uF, 6.3V, X5R	removed	

ECO15: DNP digital mic header

Can't use header at the same time as the LCD adapter board, so the part is redundant.

PVT1	PVT2	Notes
P12A JST BM04B-SRS-TB	removed	
P13A MP34DT01 (DNP)	removed	
C33A 0.1uF, 6.3V, X5R	removed	
R31A 100, 1% (DNP)	removed	
R34A 100, 1% (DNP)	removed	

ECO16: DNP backside switch

Backside user switch is not used in this configuration. Remove.

PVT1	PVT2	Notes
SW11S TL3342F160QG/TR	SW11S TL3342F160QG/TR (DNP)	

ECO17: USB hub resets

Sometimes the USB hubs don't reset nicely across soft-power cycles. Wire up hard resets to the CPU so during power on the hubs can be properly reset.

DI0_PIN4 / ball P25 is USB_HUB1_RST (most upstream hub)

DISP0_DAT6 / ball R23 is USB_HUB2_RST (most downstream hub)

Further validation indicates resetting the hubs has dubious value, so wire these using DNP 0 ohm resistors so this is a stuff option, but not actually implemented in the run

Reset lines also have pull-ups added to them, so in case they float they go to a sane value.

PVT1	PVT2	Notes
added	R23U 0 ohm	
added	R27U 0 ohm (DNP)	footprint only, not populated
added	R26U 1k, 1%	
added	R44U 0 ohm	
added	R46U 0 ohm (DNP)	footprint only, not populated
added	R45U 1k, 1%	

ECO18: Power LED turn-off

Power LED cannot be turned off currently as it monitors the 2.5V line, and during suspend this stays on.

Rewire LED to go to P1.8V_VGEN4, which is currently an unused LDO output from the regulator. Change color to red so it still turns on (dimly) at 1.8V. LED can then be powered off finally by configuring the LDO once the kernel is up and running.

The power LED is important because the LCD screen doesn't turn on for several seconds after hitting the power button, and also it's impossible to distinguish between a messed up bootloader and a power failure without a power LED at boot.

PVT1	PVT2	Notes
D10P APT1608SGC green	D10P APT1608EC red	
R10P 240, 1%	R10P 49.9, 1%	adjust current limit down

ECO19: Use external RTC

RTC drains a lot higher current than 4uA according to spec sheet.

Introduce an alternate RTC to provide time. Eliminate supercap for LICELL, as we're not using that line anymore.

We use the same RTC as on the Hummingboard.

PVT1	PVT2	Notes
C21P 0.06F 3.3V coin supercap	removed	
added	R20P 1k, 1% (DNP)	footprint added but no BOM change
added	R21P 1k, 1%	
added	Y10P Abracon ABS06-32.768KHZ-T	
added	U10P PCF8523T/1	
added	C61P 4.7uF, 10V, X5R, 10%	
added	BT11P BR1225A/FAN	

ECO20: Eliminate redundant CM chokes

L15U and L12U are ineffective and cause yield issues. Remove.

PVT1	PVT2	Notes
L15U Bournes SRF2012-900Y or equiv.	removed	
L12U Bournes SRF2012-900Y or equiv.	removed	

ECO21: Add IRQ line to Senoko

This helps simplify getting the host's attention because it's too hard to write a console driver in kernel space that listens to the UART interface for alerts.

GPT_CLKIN is repurposed to run to the Senoko header. This means you can't use the high-resolution timing feature with UART3 at the same time as the battery board, which is probably an obscure enough

combination that maybe only one person might complain about that.

PVT1	PVT2	Notes
added	R40N 330, 1%	